1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
10		643852	ENGINEERING RELEASED	10/30/08	?

SCHEMATIC,GINSU(K51)

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Preliminary

LAST_MODIFIED=Thu Oct 30 17:51:22 2008

DRAWING
TITLE=K51
ABBREV=DRAWING
LAST_MODIFIED=Thu Oct 30 17:51:22 2008

DIMENSIONS ARE IN MILLIMETERS
XX ± ____
X.XX ± ____
X.XXX ± ____
ANGLES ± ____
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

APPLE INC.

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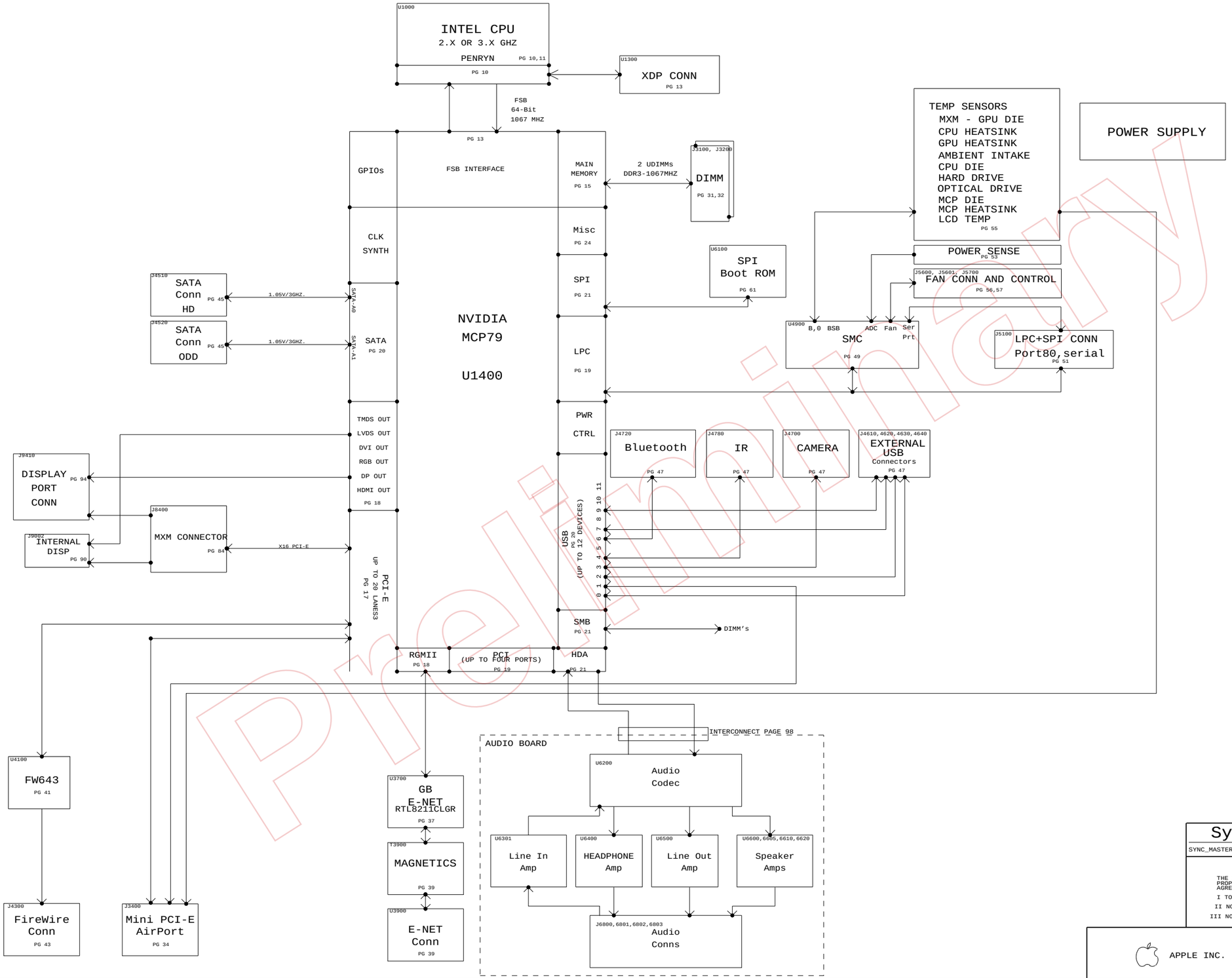
TITLE
SCH,K51,MLB

DRAWING NUMBER 051-7840 REV. 10

DRAWING SHT 1 OF 109



Preliminary

System Block Diagram

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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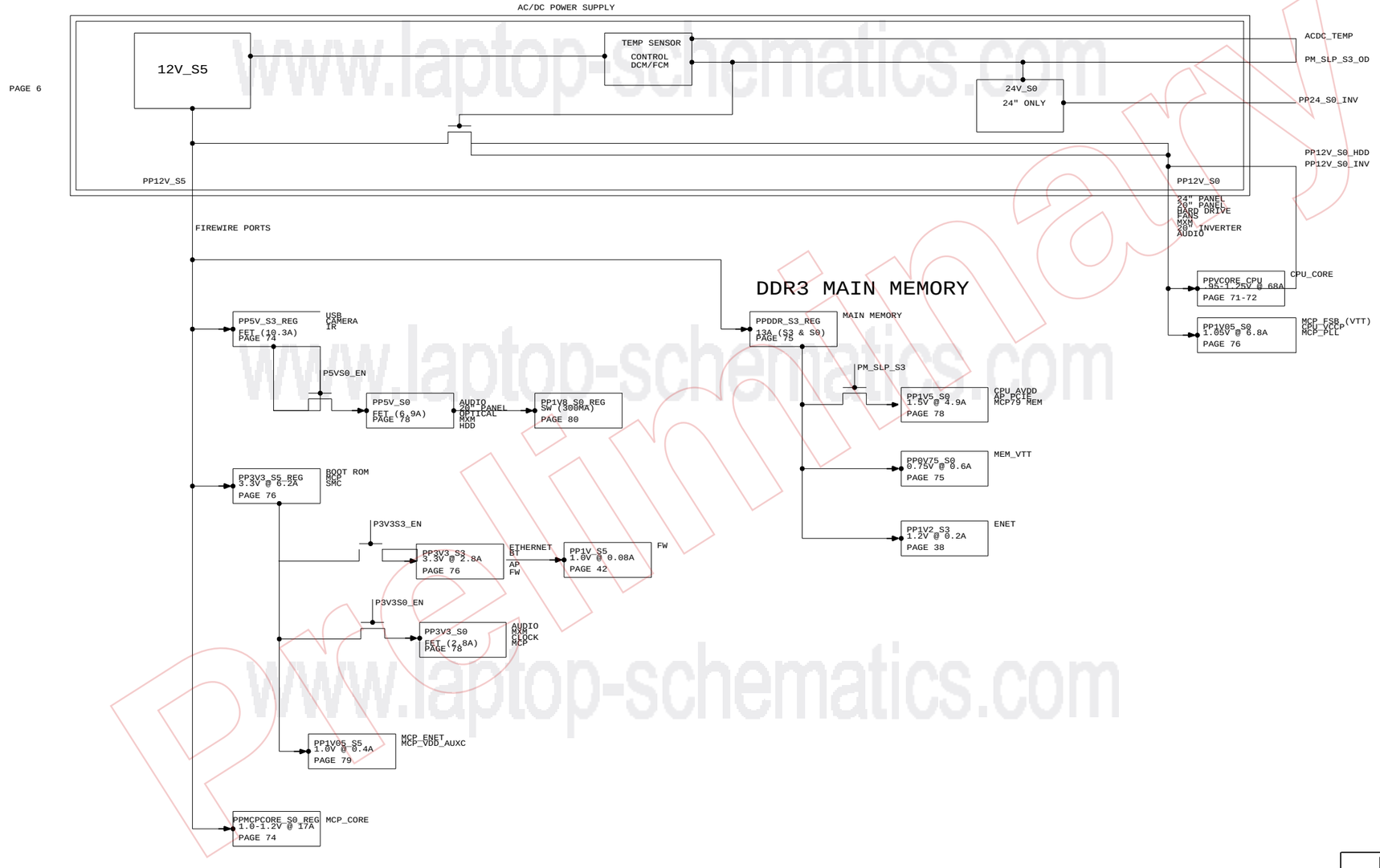
SIZE	DRAWING NUMBER	REV.
D	051-7840	10
SCALE: NONE	SHT 2 OF 109	



Preliminary
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Power Block Diagram

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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SIZE	DRAWING NUMBER	REV.
D	051-7840	10
SCALE: NONE	SHT 3 OF 109	

BOM NUMBER	BOM NAME	BOM OPTIONS
630-9765	PCBA,MLB,K51,BETTER	24_INCH_LCD,2P66GHZ_CPU,BASIC,IG
630-9773	PCBA,MLB,K51,BEST	24_INCH_LCD,2P93GHZ_CPU,BASIC,MXM,MXM_PWR_SENSE,12V_PWR_SENSE,24_INCH_MXM
630-9774	PCBA,MLB,K51,CTO_ULT	24_INCH_LCD,3P06GHZ_CPU,BASIC,MXM,MXM_PWR_SENSE,12V_PWR_SENSE,24_INCH_MXM
607-4252	K51 MLB DEVELOPMENT	DEVELOPMENT,XDP_CONN,LPCPLUS,VREFMRGN,MCP_PWR_SENSE

BOM GROUPS

BOM GROUP	BOM OPTIONS
BASIC	COMMON,ALTERNATE,MCP_TDIODE,MCP79,CPUV_PHASE3,XDP,CPU_TDIODE,MCP_B02
MCP79	BOOT_MODE_USER,MEMRESET_HW,MEMRESET_MCP

CPUS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S3698	1	IC,PDC,QJTC,QS,2.66,55W,1066,E0,6M,PGA	CPU	CRITICAL	2P66GHZ_CPU
337S3699	1	IC,PDC,QJEX,QS,2.8,55W,1066,E0,6M,PGA	CPU	CRITICAL	2P8GHZ_CPU
337S3700	1	IC,PDC,QJTF,QS,2.93,55W,1066,E0,6M,PGA	CPU	CRITICAL	2P93GHZ_CPU
337S3701	1	IC,PDC,QJTJ,QS,3.06,55W,1066,E0,6M,PGA	CPU	CRITICAL	3P06GHZ_CPU

BOARD STACK-UP

TOP	SIGNAL
2	GROUND
3	SIGNAL
4	POWER
5	POWER
6	SIGNAL
7	GROUND
BOTTOM	SIGNAL

COMMON (DELETED HDCP ROM)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0636	1	IC,GMCP,MCP79-B02,35X35MM, BGA1437, DT	U1400	CRITICAL	MCP_B02
338S0654	1	IC,FW643-06,1394B, REV-E	U4100	CRITICAL	
820-2404	1	PCB,FAB,IO ALIGNMENT,K50/K51	IO1	CRITICAL	
825-7122	1	MLB LABEL,48.0X4.8	X14	CRITICAL	
341T0135	1	EFI ROM,K50/K51	U6100	CRITICAL	
511S0038	1	CONN,INTEL SKT-P, BGA,26X26-479	U1000	CRITICAL	
338S0570	1	IC,RTL8211CL,GIGE TRANSCEIVER, 48P TQFP	U3700	CRITICAL	

K51 PARTS

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
	051-7840	1	PCB,SCHEM,MLB,K51	SCH1		24_INCH_LCD
	820-2491	1	PCB,FAB,MLB,K51,HF	MLB1		24_INCH_LCD
(338S0563 - BLNK)	341T0164	1	IC,SMC,K51	U4900	CRITICAL	24_INCH_LCD
	114S0308	1	RES,8.45K,0402,1%,1/16W,LF	R7117		24_INCH_LCD
	132S0010	1	CAP,CER,390PF,10%,50V,0402	C7113		24_INCH_LCD
	132S0178	1	CAP,CER,0.47UF,10%,6.3V,0402	C7128		24_INCH_LCD
	132S0082	1	CAP,CER,0.068UF,10%,10V,0402	C7134		24_INCH_LCD

ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
516S0657	988-2127		J3100,J3200	CONN,RCPT,SO-DIMM,DDR3,R/A,204P,LF (NON-HF)

Preliminary
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BOM Configuration

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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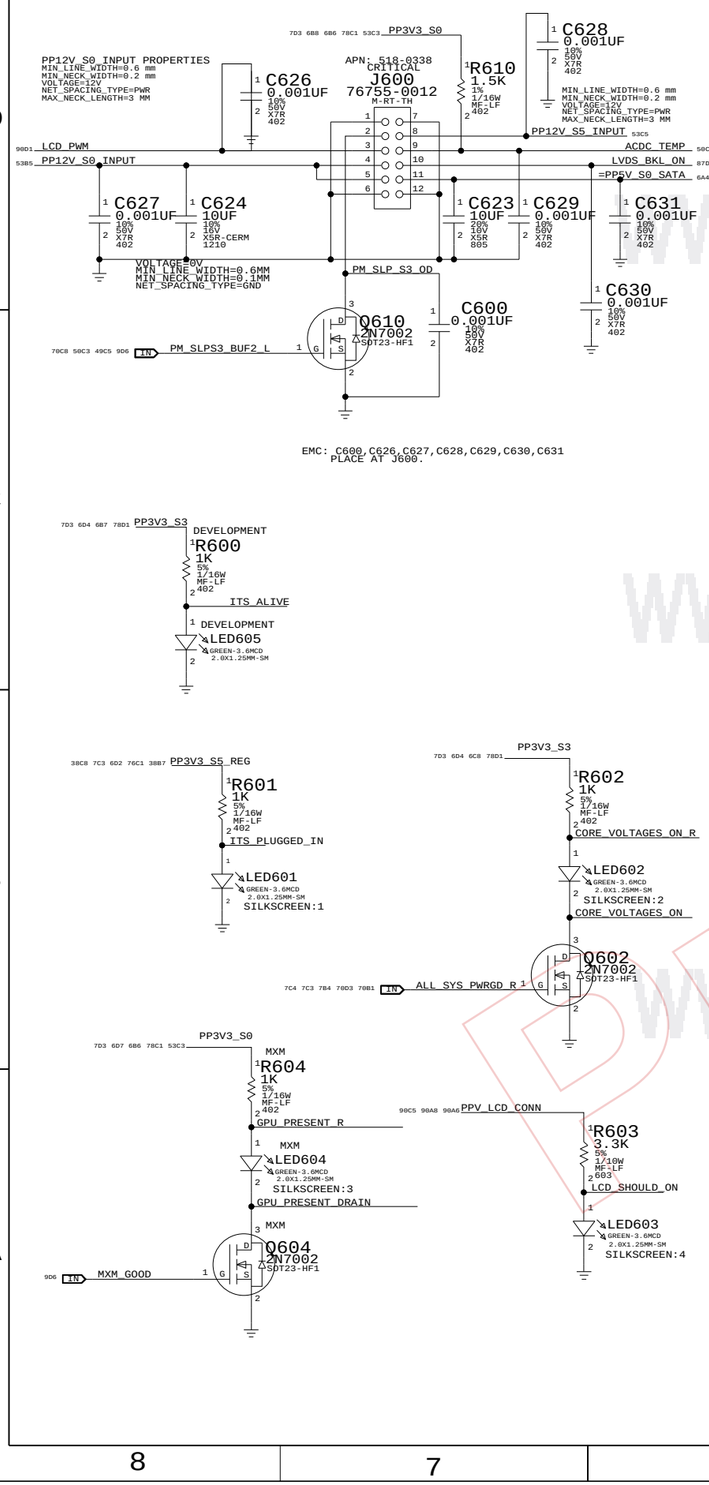
D	051-7840	10

SCALE	SHT	OF
NONE	4	109



"S0" RAILS

ONLY ON IN RUN

PPVTT_S0_DDR_LDO
MAKE_BASE=TRUE
VOLTAGE=0.75V
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP0V75_S0_MEM_VTT_A
=PP0V75_S0_MEM_VTT_B
=PPVTT_S0_VTTCLAMP

PPVCORE_CPU
MAKE_BASE=TRUE
VOLTAGE=1.25V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.3MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PPVCORE_S0_CPU

PPMCPCORE_S0_REG
MAKE_BASE=TRUE
VOLTAGE=1.05V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PPVCORE_S0_MCP

PP1V05_S0_REG
MAKE_BASE=TRUE
VOLTAGE=1.05V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP1V05_S0_MCP_FSB
=PP1V05_S0_CPU
=PP1V05_S0_MCP_AVDD_UF
=PP1V05_S0_MCP_PEX_DVDD
=PP1V05_S0_MCP_PLL_UF
=PP1V05_S0_MCP_SATA_DVDD0
=PP1V05_S0_MCP_HDMI_VDD_R

PP1V5_S0
MAKE_BASE=TRUE
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP1V5_S0_CPU
=PP1V5_S0_MINI
=PP1V8R1V5_S0_MCP_MEM

PP1V8_S0_REG
MAKE_BASE=TRUE
VOLTAGE=0V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.1MM
NET_SPACING_TYPE=GND
MAX_NECK_LENGTH=4.1 MM
=PP3V3R1V8_S0_MCP_IFP_VDD_R
=PP1V8_S0_PGCMP

PP3V3_S0
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP3V3_S0_FAN
=PP3V3_S0_MCP
=PP3V3_S0_MCP_VPLL_UF
=PP3V3_S0_MCP_GPIO
=PP3V3_S0_MCP_PLL_UF
=PP3V3R1V5_S0_MCP_HDA
=PPSPD_S0_MEM_A
=PPSPD_S0_MEM_B
=PP3V3_S0_IMVP
=PP3V3_S0_AUDIO
=PP3V3_S0_LPCPLUS
=PP3V3_S0_SMBUS
=PP3V3_S0_SMC_LS
=PP3V3_S0_SMBUS_SMC_0_S0
=PP3V3_S0_SMBUS_SMC_B_S0
=PP3V3_S0_SMBUS_SMC_MGMT
=PP3V3_S0_DPCONN
=PP3V3_S0_TSENS
=PP3V3_S0_MXM
=PP3V3_S0_XDP
=PP3V3_S0_ODD
=PP3V3_S0_SATALED
=PP3V3_S0_SMC
=PP3V3_S0_PWRCTL
=PP3V3_S0_MCPTHMSNS
=PP3V3_S0_VIDEO

PP5V_S0
MAKE_BASE=TRUE
VOLTAGE=5V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP5V_S0_LPCPLUS
=PP5V_S0_AUDIO
=PP5V_S0_SATA
=PP5V_S0_MXM
=PP5V_S0_IMVP
=PP5V_S0_DP_AUX_MUX
=PP5V_S0_1V8

PP12V_S0
MAKE_BASE=TRUE
VOLTAGE=5V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP12V_S0_FAN
=PP12V_S0_AUDIO_SPKRAMP
=PP12V_S0_CPU
=PPV_S0_MXM_PWR
=PPVIN_S0_P1V05S0
=PPV_S0_LCD_24INCH
=PPVIN_S0_MCPCORE

"S3" RAILS

ON IN RUN AND SLEEP

PPDDR_S3_REG
MAKE_BASE=TRUE
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PPDDR_MEM
MAX_NECK_LENGTH=3 MM
=PP1V5_S3_MEM_A
=PP1V5_S3_MEM_B
=PP1V5_S3_MEMRESET
=PPDDR_S3_S0FET
=PPDDR_S3_PGCMP

PPVTT_S3_DDR_BUF
MAKE_BASE=TRUE
VOLTAGE=0.75V
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 mm
=PPVTT_S3_DDR_BUF

PP3V3_S3
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP3V3_S3_MINI
=PP3V3_S3_BT
=PP3V3_S3_VREFMRGN
=PP3V3_FW_FWPHY
=PP3V3_S3_MCP_GPIO
=PP3V3_S3_SMC
=PP3V3_S3_SMBUS_SMC_A_S3
=PP3V3_S3_MCPREG

PP5V_S3_REG
MAKE_BASE=TRUE
VOLTAGE=5V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP5V_S3_BNDI
=PP5V_S3_DDRREG
=PP5V_S3_USB
=PP5V_S3_VTTCLAMP
=PP5V_S3_PWRCTL
=PP5V_S3_S0FET
=PP5V_S3_MCPREG

"S5" RAILS

ALWAYS ON WHEN UNIT HAS AC POWER (TRICKLE)

PP1V05_S5_REG
MAKE_BASE=TRUE
VOLTAGE=1.05V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP1V05_S5_MCP_VDD_AUXC

PP3V3_S5_REG
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP3V3_S5_MCP
=PP3V3_S5_MCP_GPIO
=PP3V3_S5_SMC
=PP3V3_S5_ROM
=PP3V3_S5_RTC_D
=PP3V3_S5_LPCPLUS
=PP3V3_S5_SMBUS_SMC_BSA
=PP3V3_S5_FAN
=PP3V3_S5_SMCUSBMUX
=PP3V3_S5_MEMRESET
=PP3V3_S5_P1V05S5
=PP3V3_S5_PWRCTL
=PP3V3_S5_S3FET
=PP3V3_S5_S0FET

PP5V_S5_LDO
MAKE_BASE=TRUE
VOLTAGE=5V
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP5V_S5_AVREF

PP12V_S5
MAKE_BASE=TRUE
VOLTAGE=12V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP12V_S5_FW
=PPVIN_S5_DDRREG
=PPVIN_S5_P3V3S5
=PPVIN_S5_P5VS3
=PP12V_S5_REG
=PP12V_S5_PWRCTL

Power Conn / Alias

SYNC_MASTER=K51 SYNC_DATE=04/08/2008

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D	051-7840	10
SCALE	SHT	OF
NONE	6	109

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FUNCTIONAL TESTPOINTS FOR MAC-1 & ICT

LAYOUT NOTE: PLACE NEAR J1000

FSB_A_L<6>	PP1000	OMIT	P4MM
FSB_ADSTB_L<0>	PP1001	OMIT	P4MM
FSB_A_L<27>	PP1002	OMIT	P4MM
FSB_ADSTB_L<1>	PP1003	OMIT	P4MM
FSB_D_L<0>	PP1004	OMIT	P4MM
FSB_DSTB_L_P<0>	PP1006	OMIT	P4MM
FSB_DINV_L<0>	PP1007	OMIT	P4MM
FSB_D_L<16>	PP1008	OMIT	P4MM
FSB_DSTB_L_P<1>	PP1010	OMIT	P4MM
FSB_D_L<41>	PP1012	OMIT	P4MM
FSB_DSTB_L_N<2>	PP1013	OMIT	P4MM
FSB_DINV_L<2>	PP1015	OMIT	P4MM
FSB_D_L<59>	PP1016	OMIT	P4MM
FSB_DSTB_L_N<3>	PP1017	OMIT	P4MM
FSB_DINV_L<3>	PP1019	OMIT	P4MM
CPU_INIT_L	PP1022	OMIT	P4MM
CPU_A20M_L	PP1023	OMIT	P4MM
CPU_IGNNE_L	PP1024	OMIT	P4MM
CPU_STPCLK_L	PP1025	OMIT	P4MM
CPU_INTR	PP1026	OMIT	P4MM
CPU_NMI	PP1027	OMIT	P4MM
CPU_SMI_L	PP1028	OMIT	P4MM
FSB_REQ_L<0>	PP1029	OMIT	P4MM
FSB_REQ_L<1>	PP1030	OMIT	P4MM
FSB_REQ_L<2>	PP1031	OMIT	P4MM
FSB_REQ_L<3>	PP1032	OMIT	P4MM
FSB_REQ_L<4>	PP1033	OMIT	P4MM
FSB_CLK_CPU_P	PP1034	OMIT	P4MM
FSB_CLK_CPU_N	PP1035	OMIT	P4MM

LAYOUT NOTE: PLACE NEAR U1400

FSB_A_L<6>	PP1400	OMIT	P4MM
FSB_ADSTB_L<0>	PP1401	OMIT	P4MM
FSB_A_L<27>	PP1402	OMIT	P4MM
FSB_ADSTB_L<1>	PP1403	OMIT	P4MM
FSB_D_L<0>	PP1404	OMIT	P4MM
FSB_DSTB_L_P<0>	PP1406	OMIT	P4MM
FSB_DINV_L<0>	PP1407	OMIT	P4MM
FSB_D_L<16>	PP1408	OMIT	P4MM
FSB_DSTB_L_P<1>	PP1410	OMIT	P4MM
FSB_D_L<41>	PP1412	OMIT	P4MM
FSB_DSTB_L_N<2>	PP1413	OMIT	P4MM
FSB_DINV_L<2>	PP1415	OMIT	P4MM
FSB_D_L<59>	PP1416	OMIT	P4MM
FSB_DSTB_L_N<3>	PP1417	OMIT	P4MM
FSB_DINV_L<3>	PP1419	OMIT	P4MM
FSB_LOCK_L	PP1420	OMIT	P4MM
FSB_HIT_L	PP1421	OMIT	P4MM
FSB_HITM_L	PP1422	OMIT	P4MM
FSB_BNR_L	PP1423	OMIT	P4MM
FSB_BREQ0_L	PP1424	OMIT	P4MM
FSB_DBSY_L	PP1425	OMIT	P4MM
FSB_DPWR_L	PP1426	OMIT	P4MM
FSB_REQ_L<0>	PP1427	OMIT	P4MM
FSB_REQ_L<1>	PP1428	OMIT	P4MM
FSB_REQ_L<2>	PP1429	OMIT	P4MM
FSB_REQ_L<3>	PP1430	OMIT	P4MM
FSB_REQ_L<4>	PP1431	OMIT	P4MM
VR_PWRGOOD_DELAY	PP1434	OMIT	P4MM

LAYOUT NOTE: PLACE NEAR U3700

ENET_RESET_L	PP3704	OMIT	P4MM

LAYOUT NOTE: PLACE NEAR U4100

PCIE_CLK100M_FW_P	PP4000	OMIT	P4MM
PCIE_CLK100M_FW_N	PP4001	OMIT	P4MM
PCIE_FW_R2D_P	PP4002	OMIT	P4MM
PCIE_FW_R2D_N	PP4003	OMIT	P4MM
FW_RESET_L	PP4004	OMIT	P4MM

LAYOUT NOTE: PLACE NEAR U4900

SMC_LRESET_L	PP4901	OMIT	P4MM
SMC_RESET_L	PP4902	OMIT	P4MM
LPC_AD<1>	PP4903	OMIT	P4MM

LAYOUT NOTE: PLACE NEAR U1400

PCIE_MINI_D2R_P	PP2105	OMIT	P4MM
PCIE_MINI_D2R_N	PP2106	OMIT	P4MM
PCIE_FW_D2R_P	PP2132	OMIT	P4MM
PCIE_FW_D2R_N	PP2133	OMIT	P4MM
PM_SYSRST_L	PP2113	OMIT	P4MM
PM_CLKRUN_L	PP2114	OMIT	P4MM
SATA_ODD_D2R_P	PP4904	OMIT	P4MM
SATA_ODD_D2R_N	PP4905	OMIT	P4MM
SATA_HDD_D2R_P	PP2119	OMIT	P4MM
SATA_HDD_D2R_N	PP2120	OMIT	P4MM
LPC_AD<1>	PP2121	OMIT	P4MM
USB_CAMERA_P	PP2122	OMIT	P4MM
USB_CAMERA_N	PP2123	OMIT	P4MM
USB_BT_P	PP2126	OMIT	P4MM
USB_BT_N	PP2127	OMIT	P4MM
SPI_CLK_R	PP2128	OMIT	P4MM
SPI_MISO	PP2129	OMIT	P4MM

MEM_A_DQ<7>	PP1442	OMIT	P4MM
MEM_A_DQ<14>	PP1443	OMIT	P4MM
MEM_A_DQ<16>	PP1444	OMIT	P4MM
MEM_A_DQ<25>	PP1445	OMIT	P4MM
MEM_A_DQ<47>	PP1447	OMIT	P4MM
MEM_A_DQ<59>	PP1449	OMIT	P4MM
MEM_A_DQS_P<1>	PP1452	OMIT	P4MM
MEM_A_DQS_P<2>	PP1454	OMIT	P4MM
MEM_A_DQS_P<3>	PP1456	OMIT	P4MM
MEM_A_DQS_P<4>	PP1458	OMIT	P4MM
MEM_A_DQS_P<5>	PP1460	OMIT	P4MM
MEM_A_DQS_N<6>	PP1463	OMIT	P4MM
MEM_B_DQ<6>	PP1466	OMIT	P4MM
MEM_B_DQ<8>	PP1467	OMIT	P4MM
MEM_B_DQ<23>	PP1468	OMIT	P4MM
MEM_B_DQ<25>	PP1469	OMIT	P4MM
MEM_B_DQ<38>	PP1470	OMIT	P4MM
MEM_B_DQ<62>	PP1473	OMIT	P4MM
MEM_B_DQS_P<2>	PP1478	OMIT	P4MM
MEM_B_DQS_N<3>	PP1481	OMIT	P4MM
MEM_B_DQS_N<4>	PP1483	OMIT	P4MM
MEM_B_DQS_P<5>	PP1484	OMIT	P4MM
MEM_B_DQS_N<5>	PP1485	OMIT	P4MM
MEM_B_DQS_P<6>	PP1486	OMIT	P4MM
MEM_B_DQS_N<7>	PP1489	OMIT	P4MM
PEG_D2R_P<7>	PP1490	OMIT	P4MM
PEG_D2R_N<7>	PP1491	OMIT	P4MM

LPC CONNECTOR

=PP3V3_S5_LPCPLUS	IN	FUNC_TEST=TRUE
=PP5V_S0_LPCPLUS	IN	FUNC_TEST=TRUE
LPC_CLK33M_LPCPLUS	IN	FUNC_TEST=TRUE
LPC_AD<0>	IN	FUNC_TEST=TRUE
LPC_AD<1>	IN	FUNC_TEST=TRUE
LPC_AD<2>	IN	FUNC_TEST=TRUE
LPC_AD<3>	IN	FUNC_TEST=TRUE
LPC_FRAME_L	IN	FUNC_TEST=TRUE
PM_CLKRUN_L	IN	FUNC_TEST=TRUE
SMC_TMS	IN	FUNC_TEST=TRUE
DEBUG_RESET_L	IN	FUNC_TEST=TRUE
SMC_TRST_L	IN	FUNC_TEST=TRUE
SMC_TDO	IN	FUNC_TEST=TRUE
SMC_MD1	IN	FUNC_TEST=TRUE
SMC_TX_L	IN	FUNC_TEST=TRUE
LPC_SERIRQ	IN	FUNC_TEST=TRUE
SMC_TDI	IN	FUNC_TEST=TRUE
SMC_TCK	IN	FUNC_TEST=TRUE
SMC_RESET_L	IN	FUNC_TEST=TRUE
SMC_NMI	IN	FUNC_TEST=TRUE
SMC_RX_L	IN	FUNC_TEST=TRUE
LPC_PWRDWN_L	IN	FUNC_TEST=TRUE
LPCPLUS_GPIO	IN	FUNC_TEST=TRUE
SPI_ALT_CLK	IN	FUNC_TEST=TRUE
SPI_ALT_CS_L	IN	FUNC_TEST=TRUE
SPI_ALT_MOSI	IN	FUNC_TEST=TRUE
SPI_ALT_MISO	IN	FUNC_TEST=TRUE
SPIROM_USE_MLB	IN	FUNC_TEST=TRUE
GND 16 TP'S	IN	FUNC_TEST=TRUE

MIN_ALLOWED_TPS=16

PWROK SEQUENCING

ALL_SYS_PWRGD_R	IN	FUNC_TEST=TRUE

STARTUP (BOOT/WAKE) TIMING

IMVP_VR_ON	IN	FUNC_TEST=TRUE
VR_PWRGOOD_DELAY	IN	FUNC_TEST=TRUE

SHUTDOWN/SLEEP TIMING

PM_SLP_S3_L	IN	FUNC_TEST=TRUE
PM_SLP_S4_L	IN	FUNC_TEST=TRUE
ALL_SYS_PWRGD_R	IN	FUNC_TEST=TRUE
CPU_PWRGD	IN	FUNC_TEST=TRUE

XDP CONNECTOR

XDP_BPM_L<5..0>	IN	FUNC_TEST=TRUE
TP_XDP_OBSFN_B0	IN	FUNC_TEST=TRUE
TP_XDP_OBSFN_B1	IN	FUNC_TEST=TRUE
TP_XDP_OBSDATA_B0	IN	FUNC_TEST=TRUE
TP_XDP_OBSDATA_B1	IN	FUNC_TEST=TRUE
TP_XDP_OBSDATA_B2	IN	FUNC_TEST=TRUE
TP_XDP_OBSDATA_B3	IN	FUNC_TEST=TRUE
XDP_PWRGD	IN	FUNC_TEST=TRUE
PM_LATRIGGER_L	IN	FUNC_TEST=TRUE
SMBUS_MCP_0_DATA	IN	FUNC_TEST=TRUE
SMBUS_MCP_0_CLK	IN	FUNC_TEST=TRUE
MCP_DEBUG<0..7>	IN	FUNC_TEST=TRUE
FSB_CLK_ITP_P	IN	FUNC_TEST=TRUE
FSB_CLK_ITP_N	IN	FUNC_TEST=TRUE
XDP_CPURST_L	IN	FUNC_TEST=TRUE
XDP_DBRESET_L	IN	FUNC_TEST=TRUE
XDP_TRST_L	IN	FUNC_TEST=TRUE
XDP_TDI	IN	FUNC_TEST=TRUE
XDP_TMS	IN	FUNC_TEST=TRUE
XDP_TDO	IN	FUNC_TEST=TRUE
XDP_TCK	IN	FUNC_TEST=TRUE
JTAG_MCP_TDI	IN	FUNC_TEST=TRUE
JTAG_MCP_TMS	IN	FUNC_TEST=TRUE
JTAG_MCP_TCK	IN	FUNC_TEST=TRUE
JTAG_MCP_TDO	IN	FUNC_TEST=TRUE
JTAG_MCP_TRST_L	IN	FUNC_TEST=TRUE

"S0" RAILS

10 TP'S

PPVTT_S0_DDR_LDO	IN	FUNC_TEST=TRUE
PPVCORE_CPU	IN	FUNC_TEST=TRUE
PPMCPCORE_S0_REG	IN	FUNC_TEST=TRUE
PP1V05_S0_REG	IN	FUNC_TEST=TRUE
PP1V5_S0	IN	FUNC_TEST=TRUE
PP1V8_S0_REG	IN	FUNC_TEST=TRUE
PP3V3_S0	IN	FUNC_TEST=TRUE
PP5V_S0	IN	FUNC_TEST=TRUE
PP12V_S0	IN	FUNC_TEST=TRUE

"S3" RAILS

4 TP'S

PPDDR_S3_REG	IN	FUNC_TEST=TRUE
PPVTT_S3_DDR_BUF	IN	FUNC_TEST=TRUE
PP3V3_S3	IN	FUNC_TEST=TRUE
PP5V_S3_REG	IN	FUNC_TEST=TRUE

"S5" RAILS

3 TP'S

PP1V05_S5_REG	IN	FUNC_TEST=TRUE
PP3V3_S5_REG	IN	FUNC_TEST=TRUE
PP5V_S5_LDO	IN	FUNC_TEST=TRUE
PP12V_S5	IN	FUNC_TEST=TRUE

PM_SYSRST_L	IN	FUNC_TEST=TRUE
SMC_MANUAL_RST_L	IN	FUNC_TEST=TRUE
ALL_SYS_PWRGD_R	IN	FUNC_TEST=TRUE

FOR ICT

GPU_CLK100M_PCIE_N	IN	FUNC_TEST=TRUE
FSB_CLK_CPU_N	IN	FUNC_TEST=TRUE
PCI_REQ0_L	IN	FUNC_TEST=TRUE
PCI_REQ1_L	IN	FUNC_TEST=TRUE
TP_FW643_TCK	IN	FUNC_TEST=TRUE
TP_FW643_TMS	IN	FUNC_TEST=TRUE
TP_FW643_TDI	IN	FUNC_TEST=TRUE
TP_FW643_TDO	IN	FUNC_TEST=TRUE
TP_FW643_SM	IN	FUNC_TEST=TRUE
TP_FW643_SE	IN	FUNC_TEST=TRUE
TP_FW643_NAND_TREE	IN	FUNC_TEST=TRUE
TP_FW643_CE	IN	FUNC_TEST=TRUE
FW_RESET_L	IN	FUNC_TEST=TRUE

MISC GROUND VIAS

ZH500 HOLE-VIA, ZH501 HOLE-VIA, ZH502 HOLE-VIA, ZH503 HOLE-VIA, ZH504 HOLE-VIA, ZH505 HOLE-VIA, ZH506 HOLE-VIA, ZH507 HOLE-VIA, ZH508 HOLE-VIA, ZH509 HOLE-VIA, ZH510 HOLE-VIA, ZH511 HOLE-VIA, ZH512 HOLE-VIA, ZH513 HOLE-VIA, ZH514 HOLE-VIA, ZH515 HOLE-VIA, ZH516 HOLE-VIA, ZH517 HOLE-VIA, ZH518 HOLE-VIA, ZH519 HOLE-VIA, ZH520 HOLE-VIA, ZH521 HOLE-VIA, ZH522 HOLE-VIA, ZH523 HOLE-VIA, ZH524 HOLE-VIA, ZH525 HOLE-VIA, ZH526 HOLE-VIA, ZH527 HOLE-VIA, ZH528 HOLE-VIA, ZH529 HOLE-VIA, ZH531 HOLE-VIA, ZH532 HOLE-VIA, ZH534 HOLE-VIA, ZH535 HOLE-VIA, ZH536 HOLE-VIA, ZH537 HOLE-VIA

CRITICAL
SC0700 EMI-SPRING CLIP-SM1
SC0701 EMI-SPRING CLIP-SM1
CRITICAL BTW DIMMS
SC0702 EMI-SPRING CLIP-SM-K2

835-0266
CRITICAL SDF0726 NUT-6.5OD1.8H-1.56-3.8-TH
CRITICAL SDF0727 NUT-6.5OD1.8H-1.56-3.8-TH

998-0846 FOR MCP HEATSINK
ZH0722 4R3P25, ZH0723 4R3P25, ZH0725 4R3P25, ZH0730 4R3P25

998-0850
ZH0700 4P75R4, ZH0701 4P75R4, ZH0702 4P75R4, ZH0703 4P75R4

998-0847
ZH0711 5R3P5-6B 998-1608
ZH0712 4P25R3P5, ZH0713 4P25R3P5, ZH0714 4P25R3P5, ZH0715 4P25R3P5

CRITICAL 860-0895 SDF0717 STDOFF-7P0OD15P0H-TH

998-0847
ZH0718 4P25R3P5, ZH0720 4P25R3P5

Functional / ICT Test

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7840	10
SCALE: NONE	SHT 7 OF 109	

Preliminary
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NC ON UNUSED ALIASES

18C6	MCP_TV_DAC_RSET	NC_MCP_TV_DAC_RSET	MAKE_BASE=TRUE	NO_TEST=TRUE
18C6	MCP_TV_DAC_VREF	NC_MCP_TV_DAC_VREF	MAKE_BASE=TRUE	NO_TEST=TRUE
18C6	MCP_CLK27M_XTALIN	NC_MCP_CLK27M_XTALIN	MAKE_BASE=TRUE	NO_TEST=TRUE
18C6	MCP_CLK27M_XTALOUT	NC_MCP_CLK27M_XTALOUT	MAKE_BASE=TRUE	NO_TEST=TRUE
18C3	CRT_IG_R_C_PR	NC_CRT_IG_R_C_PR	MAKE_BASE=TRUE	NO_TEST=TRUE
18C3	CRT_IG_G_Y_Y	NC_CRT_IG_G_Y_Y	MAKE_BASE=TRUE	NO_TEST=TRUE
18C3	CRT_IG_B_COMP_PB	NC_CRT_IG_B_COMP_PB	MAKE_BASE=TRUE	NO_TEST=TRUE
18C3	CRT_IG_HSYNC	NC_CRT_IG_HSYNC	MAKE_BASE=TRUE	NO_TEST=TRUE
18C3	CRT_IG_VSYNC	NC_CRT_IG_VSYNC	MAKE_BASE=TRUE	NO_TEST=TRUE
18C3	TP_MCP_RGB_HSYNC	NC_MCP_RGB_HSYNC	MAKE_BASE=TRUE	NO_TEST=TRUE
18C3	TP_MCP_RGB_VSYNC	NC_MCP_RGB_VSYNC	MAKE_BASE=TRUE	NO_TEST=TRUE
19C7	TP_PCI_AD<31..15>	NC_PCI_AD<31..15>	MAKE_BASE=TRUE	NO_TEST=TRUE
19D4	TP_PCI_IRDY_L	NC_PCI_IRDY_L	MAKE_BASE=TRUE	NO_TEST=TRUE
19D4	TP_PCI_C_BE_L<1..0>	NC_PCI_C_BE_L<1..0>	MAKE_BASE=TRUE	NO_TEST=TRUE
19D4	TP_PCI_SERR_L	NC_PCI_SERR_L	MAKE_BASE=TRUE	NO_TEST=TRUE
19D4	TP_PCI_DEVSEL_L	NC_PCI_DEVSEL_L	MAKE_BASE=TRUE	NO_TEST=TRUE
19D4	TP_PCI_PERR_L	NC_PCI_PERR_L	MAKE_BASE=TRUE	NO_TEST=TRUE
19B7	TP_LPC_DRQ0_L	NC_LPC_DRQ0_L	MAKE_BASE=TRUE	NO_TEST=TRUE
21B3	TP_MCP_BUF_SIO_CLK	NC_MCP_BUF_SIO_CLK	MAKE_BASE=TRUE	NO_TEST=TRUE
16D6	TP_MEM_A_ODT<3..2>	NC_MEM_A_ODT<3..2>	MAKE_BASE=TRUE	NO_TEST=TRUE
16D6 16C6	TP_MEM_A_CKE<3..2>	NC_MEM_A_CKE<3..2>	MAKE_BASE=TRUE	NO_TEST=TRUE
16D6	TP_MEM_A_CS_L<3..2>	NC_MEM_A_CS_L<3..2>	MAKE_BASE=TRUE	NO_TEST=TRUE
15B5	TP_MEM_A_CLK2P	NC_MEM_A_CLK2P	MAKE_BASE=TRUE	NO_TEST=TRUE
15B5	TP_MEM_A_CLK2N	NC_MEM_A_CLK2N	MAKE_BASE=TRUE	NO_TEST=TRUE
16D6	TP_MEM_A_CLK3P	NC_MEM_A_CLK3P	MAKE_BASE=TRUE	NO_TEST=TRUE
16D6	TP_MEM_A_CLK3N	NC_MEM_A_CLK3N	MAKE_BASE=TRUE	NO_TEST=TRUE
16D6	TP_MEM_A_CLK4P	NC_MEM_A_CLK4P	MAKE_BASE=TRUE	NO_TEST=TRUE
16D6	TP_MEM_A_CLK4N	NC_MEM_A_CLK4N	MAKE_BASE=TRUE	NO_TEST=TRUE
16D6	TP_MEM_A_CLK5P	NC_MEM_A_CLK5P	MAKE_BASE=TRUE	NO_TEST=TRUE
16D6	TP_MEM_A_CLK5N	NC_MEM_A_CLK5N	MAKE_BASE=TRUE	NO_TEST=TRUE
16D3	TP_MEM_B_CS_L<3..2>	NC_MEM_B_CS_L<3..2>	MAKE_BASE=TRUE	NO_TEST=TRUE
16D3	TP_MEM_B_ODT<3..2>	NC_MEM_B_ODT<3..2>	MAKE_BASE=TRUE	NO_TEST=TRUE
16D3 16C3	TP_MEM_B_CKE<3..2>	NC_MEM_B_CKE<3..2>	MAKE_BASE=TRUE	NO_TEST=TRUE
15B1	TP_MEM_B_CLK2P	NC_MEM_B_CLK2P	MAKE_BASE=TRUE	NO_TEST=TRUE
15B1	TP_MEM_B_CLK2N	NC_MEM_B_CLK2N	MAKE_BASE=TRUE	NO_TEST=TRUE
16D3	TP_MEM_B_CLK3P	NC_MEM_B_CLK3P	MAKE_BASE=TRUE	NO_TEST=TRUE
16D3	TP_MEM_B_CLK3N	NC_MEM_B_CLK3N	MAKE_BASE=TRUE	NO_TEST=TRUE
16D3	TP_MEM_B_CLK4P	NC_MEM_B_CLK4P	MAKE_BASE=TRUE	NO_TEST=TRUE
16D3	TP_MEM_B_CLK4N	NC_MEM_B_CLK4N	MAKE_BASE=TRUE	NO_TEST=TRUE
16D3	TP_MEM_B_CLK5P	NC_MEM_B_CLK5P	MAKE_BASE=TRUE	NO_TEST=TRUE
16D3	TP_MEM_B_CLK5N	NC_MEM_B_CLK5N	MAKE_BASE=TRUE	NO_TEST=TRUE

18C6	TP_ENET_INTR_L	NC_ENET_INTR_L	MAKE_BASE=TRUE	NO_TEST=TRUE
18C3	TP_ENET_PWRDWN_L	NC_ENET_PWDWN_L	MAKE_BASE=TRUE	NO_TEST=TRUE
21C7	TP_MCP_KBDRSTIN_L	NC_MCP_KBDRSTIN_L	MAKE_BASE=TRUE	NO_TEST=TRUE
17B6	TP_MCP_GPIO_18	NC_MCP_GPIO_18	MAKE_BASE=TRUE	NO_TEST=TRUE
21D7	TP_MLB_RAM_SIZE	NC_MLB_RAM_SIZE	MAKE_BASE=TRUE	NO_TEST=TRUE
19D4	TP_PCI_C_BE_L<3>	NC_PCI_C_BE_L<3>	MAKE_BASE=TRUE	NO_TEST=TRUE
19C4	TP_PCI_CLK0	NC_PCI_CLK0	MAKE_BASE=TRUE	NO_TEST=TRUE
19C4	TP_PCI_CLK1	NC_PCI_CLK1	MAKE_BASE=TRUE	NO_TEST=TRUE
19D4	TP_PCI_FRAME_L	NC_PCI_FRAME_L	MAKE_BASE=TRUE	NO_TEST=TRUE
19D4	TP_PCI_GNT0_L	NC_MCP_PCI_GNT0_L	MAKE_BASE=TRUE	NO_TEST=TRUE
19D4	TP_PCI_GNT1_L	NC_PCI_GNT1_L	MAKE_BASE=TRUE	NO_TEST=TRUE
19C7	TP_PCI_INTW_L	NC_PCI_INTW_L	MAKE_BASE=TRUE	NO_TEST=TRUE
19C7	TP_PCI_INTX_L	NC_PCI_INTX_L	MAKE_BASE=TRUE	NO_TEST=TRUE
19C7	TP_PCI_INTY_L	NC_PCI_INTY_L	MAKE_BASE=TRUE	NO_TEST=TRUE
19C7	TP_PCI_INTZ_L	NC_PCI_INTZ_L	MAKE_BASE=TRUE	NO_TEST=TRUE
19D4	TP_PCI_PAR	NC_PCI_PAR	MAKE_BASE=TRUE	NO_TEST=TRUE
19C4	TP_PCI_RESET1_L	NC_PCI_RESET1_L	MAKE_BASE=TRUE	NO_TEST=TRUE
19D4	TP_PCI_STOP_L	NC_PCI_STOP_L	MAKE_BASE=TRUE	NO_TEST=TRUE
19C7	TP_PCI_TRDY_L	NC_PCI_TRDY_L	MAKE_BASE=TRUE	NO_TEST=TRUE
17C3	TP_PCIE_CLK100M_PE4N	NC_PCIE_CLK100M_PE4N	MAKE_BASE=TRUE	NO_TEST=TRUE
17C3	TP_PCIE_CLK100M_PE4P	NC_PCIE_CLK100M_PE4P	MAKE_BASE=TRUE	NO_TEST=TRUE
17B3	TP_PCIE_CLK100M_PE5N	NC_PCIE_CLK100M_PE5N	MAKE_BASE=TRUE	NO_TEST=TRUE
17B3	TP_PCIE_CLK100M_PE5P	NC_PCIE_CLK100M_PE5P	MAKE_BASE=TRUE	NO_TEST=TRUE
17B3	TP_PCIE_CLK100M_PE6P	NC_PCIE_CLK100M_PE6P	MAKE_BASE=TRUE	NO_TEST=TRUE
17C6	PCIE_EXCARD_PRSNT_L	NC_PCIE_EXCARD_PRSNT_L	MAKE_BASE=TRUE	NO_TEST=TRUE
17C6	TP_PE4_CLKREQ_L	NC_PE4_CLKREQ_L	MAKE_BASE=TRUE	NO_TEST=TRUE
17C6	TP_PE4_PRSNT_L	NC_PE4_PRSNT_L	MAKE_BASE=TRUE	NO_TEST=TRUE
21C7	TP_SB_A20GATE	NC_SB_A20GATE	MAKE_BASE=TRUE	NO_TEST=TRUE
20C3	TP_USB_10N	NC_USB_10N	MAKE_BASE=TRUE	NO_TEST=TRUE
20C3	TP_USB_10P	NC_USB_10P	MAKE_BASE=TRUE	NO_TEST=TRUE
20C3	TP_USB_11N	NC_USB_11N	MAKE_BASE=TRUE	NO_TEST=TRUE
20C3	TP_USB_11P	NC_USB_11P	MAKE_BASE=TRUE	NO_TEST=TRUE
20C3	USB_EXCARD_N	NC_USB_EXCARD_N	MAKE_BASE=TRUE	NO_TEST=TRUE
20C3	USB_EXCARD_P	NC_USB_EXCARD_P	MAKE_BASE=TRUE	NO_TEST=TRUE
21B3	ODD_PWR_EN_L	NC_ODD_PWR_EN_L	MAKE_BASE=TRUE	NO_TEST=TRUE
17C3	PCIE_CLK100M_EXCARD_P	NC_PCIE_CLK100M_EXCARD_P	MAKE_BASE=TRUE	NO_TEST=TRUE
17C3	PCIE_CLK100M_EXCARD_N	NC_PCIE_CLK100M_EXCARD_N	MAKE_BASE=TRUE	NO_TEST=TRUE
17C6	EXCARD_CLKREQ_L	NC_EXCARD_CLKREQ_L	MAKE_BASE=TRUE	NO_TEST=TRUE
19D7	TP_PCI_AD<12..10>	NC_PCI_AD<12..10>	MAKE_BASE=TRUE	NO_TEST=TRUE
19D7	TP_PCI_AD<8>	NC_PCI_AD<8>	MAKE_BASE=TRUE	NO_TEST=TRUE

TESTPOINT ALIAS FOR UNUSED NETS

17B6	PCIE_EXCARD_D2R_P	TP_PCIE_EXCARD_D2R_P	MAKE_BASE=TRUE
17B6	PCIE_EXCARD_D2R_N	TP_PCIE_EXCARD_D2R_N	MAKE_BASE=TRUE
17B3	PCIE_EXCARD_R2D_C_P	TP_PCIE_EXCARD_R2D_C_P	MAKE_BASE=TRUE
17B3	PCIE_EXCARD_R2D_C_N	TP_PCIE_EXCARD_R2D_C_N	MAKE_BASE=TRUE
71C7	VR_PWRGD_CLKEN_L	TP_VR_PWRGD_CLKEN_L	MAKE_BASE=TRUE
90C4 90A3 6D6 87D5	LN	LVDS_BKL_ON	MAKE_BASE=TRUE

UNUSED INTERNAL USB PORTS

20D3	USB_TPAD_N	TP_USB_TPAD_N	MAKE_BASE=TRUE
20D3	USB_TPAD_P	TP_USB_TPAD_P	MAKE_BASE=TRUE

MCP HAS INTERNAL 15K PULL-DOWNS

UNUSED MEMORY SIGNALS

31D5	MEM_A_A<15>	TP_MEM_A_A<15>	MAKE_BASE=TRUE
32D5	MEM_B_A<15>	TP_MEM_B_A<15>	MAKE_BASE=TRUE

TESTPOINT FOR OPTIONAL GMUX JTAG FROM MCP

17B6	GMUX_JTAG_TCK_L	NC_GMUX_JTAG_TCK_L	MAKE_BASE=TRUE	NO_TEST=TRUE
17B6	GMUX_JTAG_TDO	NC_GMUX_JTAG_TDO	MAKE_BASE=TRUE	NO_TEST=TRUE
19D4	GMUX_JTAG_TDI	NC_GMUX_JTAG_TDI	MAKE_BASE=TRUE	NO_TEST=TRUE
19D4	GMUX_JTAG_TMS	NC_GMUX_JTAG_TMS	MAKE_BASE=TRUE	NO_TEST=TRUE

K51 ONLY STANDOFFS

CRITICAL	CRITICAL
860-0895	860-0895
SDF0800	SDF0801
STDOFF-7P0OD15P0H-TH	STDOFF-7P0OD15P0H-TH

UNUSED SIGNAL ALIAS/STAND OFF

SYNC_MASTER=K51 SYNC_DATE=04/07/2008

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D	051-7840	10
SCALE: NONE	SHT 8 OF 109	

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SIGNAL ALIAS

10B2 CPU_PSI_L == IMVP6_PSI_L (MAKE_BASE=TRUE) 71C7

21D7 TP_MLB_RAM_VENDOR == MXM_GOOD (MAKE_BASE=TRUE) 6A8

7B4 102B3 21C3 PM_SLP_S3_L — R910 15 5% 1/16W MF-LF 402 — PM_SLPS3_BUF2_L (MAKE_BASE=TRUE) 6C8 49C5 50C3 79C8

(P50 HAS A 100K TO GROUND)

R911 15 5% 1/16W MF-LF 402 — PM_SLPS3_BUF1_L (MAKE_BASE=TRUE) 73A6 94D7

R912 100K 5% 1/16W MF-LF 402

PEG Slot Support

17C3	IN	PEG_CLK100M_P == GPU_CLK100M_PCIE_P (MAKE_BASE=TRUE)	OUT	87C5 102C3
17C3	IN	PEG_CLK100M_N == GPU_CLK100M_PCIE_N (MAKE_BASE=TRUE)	OUT	87C5 102C3 7C3
17D3 17C3	IN	=PEG_R2D_C_P<0..15> == PEG_R2D_C_P<0..15> (MAKE_BASE=TRUE)	OUT	102D3 86A7 86B7 86C7 86D7
17D3 17C3	IN	=PEG_R2D_C_N<0..15> == PEG_R2D_C_N<0..15> (MAKE_BASE=TRUE)	OUT	102D3 86A7 86B7 86C7 86D7
17D6 17C6	OUT	=PEG_D2R_P<0..15> == PEG_D2R_P<0..15> (MAKE_BASE=TRUE)	IN	7B7 86A1 86B1 86C1 86D1 102D3
17D6 17C6	OUT	=PEG_D2R_N<0..15> == PEG_D2R_N<0..15> (MAKE_BASE=TRUE)	IN	7B7 86A1 86B1 86C1 86D1 102D3
17C6	IN	PEG_PRSNT_L == MXM_DETECT_L (MAKE_BASE=TRUE)	OUT	85B6 85B3

DisplayPort / TMDS Support

18B6	IN	=MCP_HDMI_TXC_P == DP_IG_ML_P<3> (MAKE_BASE=TRUE)	OUT	107D2 91C4
18B6	IN	=MCP_HDMI_TXC_N == DP_IG_ML_N<3> (MAKE_BASE=TRUE)	OUT	107D2 91D4
18B6	IN	=MCP_HDMI_TXD_P<0..2> == DP_IG_ML_P<2..0> (MAKE_BASE=TRUE)	OUT	107D2 91B7 91B8 91C8
18B6	IN	=MCP_HDMI_TXD_N<0..2> == DP_IG_ML_N<2..0> (MAKE_BASE=TRUE)	OUT	107D2 91B8 91C8 91D8
18A3	IN	=MCP_HDMI_DDC_CLK == DP_IG_DDC_CLK (MAKE_BASE=TRUE)	OUT	93C8
18A3	BI	=MCP_HDMI_DDC_DATA == DP_IG_DDC_DATA (MAKE_BASE=TRUE)	BI	93D8
18B6	OUT	=MCP_HDMI_HPD == DP_IG_HPD (MAKE_BASE=TRUE)	IN	91B4

18B6 =DVI_HPD_GMUX_INT == HPLUG_DET2 (MAKE_BASE=TRUE) — R900 20K 5% 1/16W MF-LF 402

MCP79 PCIe PRSNT# Straps

PCIE_FW_PRSNT_L OUT 17C6

PCIE_MINI_PRSNT_L OUT 17C6

USB ALIAS

70D8 PGOOD_5V_S3 IN — PM_EN_USB_PWR OUT 46C8

GROUND ALIAS

GND RAILS

98D6 GND_AUDIO_SPKRAMP — GND (MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.09MM, VOLTAGE=0V, NET_SPACING_TYPE=GND, MAKE_BASE=TRUE, MAX_NECK_LENGTH=4.1 MM)

Platform Reset Connections

LPC Reset (Unbuffered)

103D3 19C3 LPC_RESET_L IN — PLACEMENT_NOTE=Place close to U1400 — R981 33 5% 1/16W MF-LF 402 — DEBUG_RESET_L OUT 7D4 51D5

R983 33 5% 1/16W MF-LF 402 — SMC_LRESET_L OUT 7D6 49C8

PLACEMENT_NOTE=Place close to U1400

PCIE Reset (Unbuffered)

17B3 PCIE_RESET_L IN

R992 0 5% 1/16W MF-LF 402 — FW_RESET_L OUT 7D6 7B3 41A2

R991 0 5% 1/16W MF-LF 402 — MINI_RESET_L OUT 34C3

R990 0 5% 1/16W MF-LF 402 — PEG_RESET_L OUT 87C5 90D4

R971 0 5% 1/16W MF-LF 402 — PCA9557D_RESET_L OUT 29A5

19C4 MEM_VTT_EN_R IN — R972 33 5% 1/16W MF-LF 402 — DDRVTT_EN OUT 75C8 78A4

NO STUFF C973 0.47UF 10% 6.3V CERM-X5R 402

103D3 19B3 LPC_CLK33M_SMC_R IN — PLACEMENT_NOTE=Place close to U1400 — R925 33 5% 1/16W MF-LF 402 — LPC_CLK33M_SMC OUT 103D3 49C8

R926 33 5% 1/16W MF-LF 402 — LPC_CLK33M_LPCPLUS OUT 103D3 7D4 51D4

PLACEMENT_NOTE=Place close to U1400

103D3 21B3 PM_CLK32K_SUSCLK_R IN — R929 22 5% 1/16W MF-LF 402 — PM_CLK32K_SUSCLK OUT 103D3 49C5

PLACEMENT_NOTE=Place close to U1400

MCP_CPUVDD_EN WILL ASSERT AFTER MCP_PS_PWRGD IS UP

21B3 MCP_CPUVDD_EN IN — R930 22 5% 1/16W MF-LF 402 — MCP_CPU_VLD OUT 21B7

PLACEMENT_NOTE=Place close to U1400

18D6 =MCP_MII_RXER == MCP_MII_NU (MAKE_BASE=TRUE)

18D6 =MCP_MII_COL

18D6 =MCP_MII_CRS

R955 47K 5% 1/16W MF-LF 402

SIGNAL & GND ALIASES

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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SCALE: NONE	SHT 9 OF 109	

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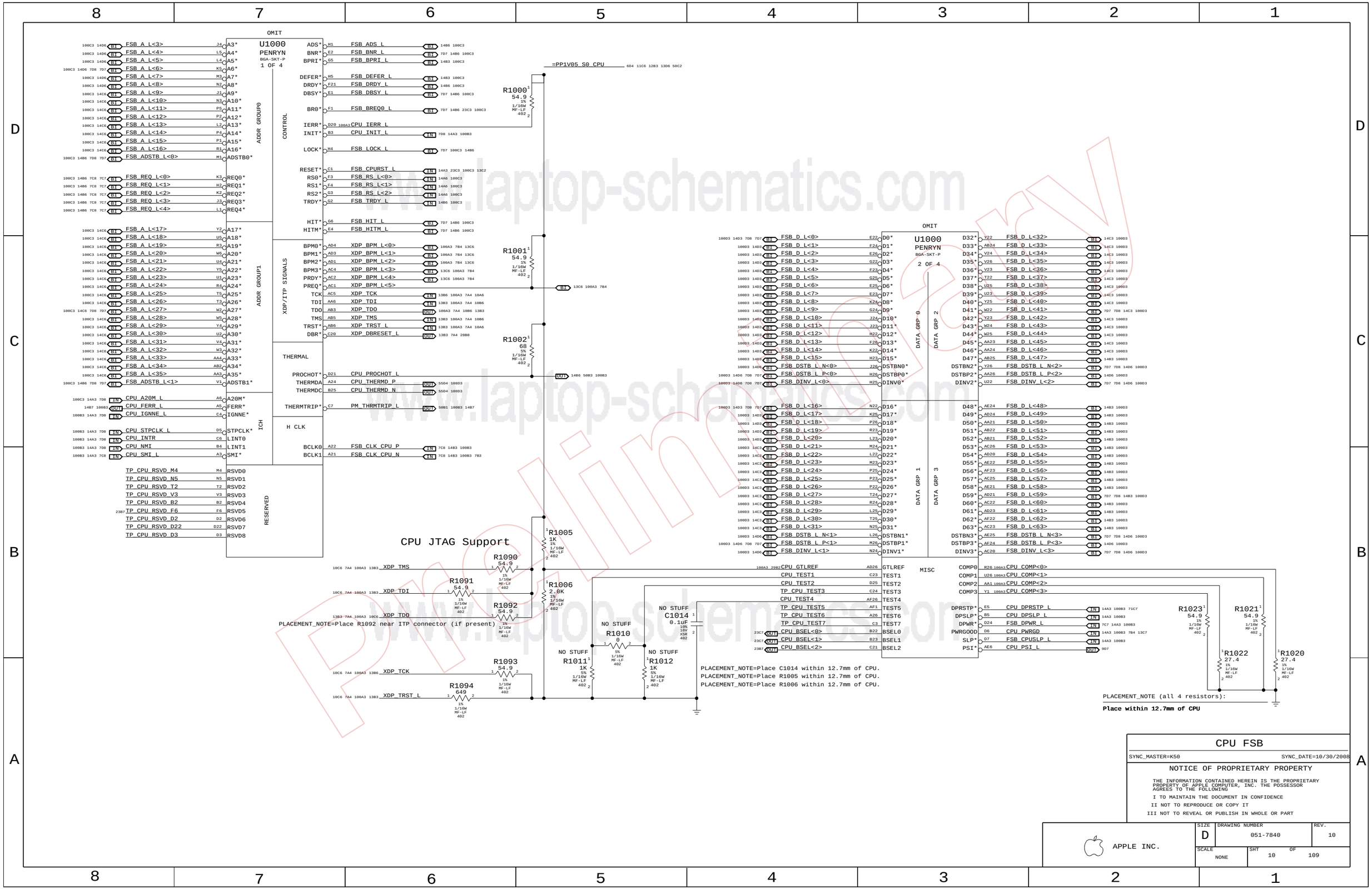
OMIT
U1000
PENRYN
BGA-SKT-P
1 OF 4
ADDR GROUP0
ADDR GROUP1
CONTROL
XDP/ITP SIGNALS
THERMAL
H CLK
ICH
RESERVED
FSB_A_L<3>
FSB_A_L<4>
FSB_A_L<5>
FSB_A_L<6>
FSB_A_L<7>
FSB_A_L<8>
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FSB_A_L<14>
FSB_A_L<15>
FSB_A_L<16>
FSB_ADSTB_L<0>
FSB_REQ_L<0>
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FSB_REQ_L<4>
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FSB_A_L<32>
FSB_A_L<33>
FSB_A_L<34>
FSB_A_L<35>
FSB_ADSTB_L<1>
CPU_A20M_L
CPU_FERR_L
CPU_IGNNE_L
CPU_STPCLK_L
CPU_INTR
CPU_NMI
CPU_SMI_L
TP_CPU_RSVD_M4
TP_CPU_RSVD_N5
TP_CPU_RSVD_T2
TP_CPU_RSVD_V3
TP_CPU_RSVD_B2
TP_CPU_RSVD_F6
TP_CPU_RSVD_D2
TP_CPU_RSVD_D22
TP_CPU_RSVD_D3
ADS*
BNR*
BPRI*
DEFER*
DRDY*
DBSY*
BR0*
IERR*
INIT*
LOCK*
RESET*
RS0*
RS1*
RS2*
TRDY*
HIT*
HITM*
BPM0*
BPM1*
BPM2*
BPM3*
PRDY*
PREQ*
TCK
TDI
TDO
TMS
TRST*
DBR*
PROCHOT*
THERMDA
THERMDC
THERMTRIP*
BCLK0
BCLK1
FSB_ADS_L
FSB_BNR_L
FSB_BPRI_L
FSB_DEFER_L
FSB_DRDY_L
FSB_DBSY_L
FSB_BREQ0_L
CPU_IERR_L
CPU_INIT_L
FSB_LOCK_L
FSB_CPURST_L
FSB_RS_L<0>
FSB_RS_L<1>
FSB_RS_L<2>
FSB_TRDY_L
FSB_HIT_L
FSB_HITM_L
XDP_BPM_L<0>
XDP_BPM_L<1>
XDP_BPM_L<2>
XDP_BPM_L<3>
XDP_BPM_L<4>
XDP_BPM_L<5>
XDP_TCK
XDP_TDI
XDP_TDO
XDP_TMS
XDP_TRST_L
XDP_DBRESET_L
CPU_PROCHOT_L
CPU_THERMD_P
CPU_THERMD_N
PM_THRMTRIP_L
FSB_CLK_CPU_P
FSB_CLK_CPU_N
=PP1V05_S0_CPU
R1000 54.9 1% 1/16W MF-LF 402
R1001 54.9 1% 1/16W MF-LF 402
R1002 68 5% 1/16W MF-LF 402
R1005 1K 1% 1/16W MF-LF 402
R1006 2.0K 1% 1/16W MF-LF 402
R1090 54.9 1% 1/16W MF-LF 402
R1091 54.9 1% 1/16W MF-LF 402
R1092 54.9 1% 1/16W MF-LF 402
R1093 54.9 1% 1/16W MF-LF 402
R1094 649 1% 1/16W MF-LF 402
R1010 0 5% 1/16W MF-LF 402
R1011 1K 5% 1/16W MF-LF 402
R1012 1K 5% 1/16W MF-LF 402
C1014 0.1uF 10% 16V X5R 402
NO STUFF
CPU JTAG Support
PLACEMENT_NOTE=Place R1092 near ITP connector (if present)
PLACEMENT_NOTE=Place C1014 within 12.7mm of CPU.
PLACEMENT_NOTE=Place R1005 within 12.7mm of CPU.
PLACEMENT_NOTE=Place R1006 within 12.7mm of CPU.
OMIT
U1000
PENRYN
BGA-SKT-P
2 OF 4
DATA GRP 0
DATA GRP 1
DATA GRP 2
DATA GRP 3
MISC
FSB_D_L<0>
FSB_D_L<1>
FSB_D_L<2>
FSB_D_L<3>
FSB_D_L<4>
FSB_D_L<5>
FSB_D_L<6>
FSB_D_L<7>
FSB_D_L<8>
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FSB_D_L<10>
FSB_D_L<11>
FSB_D_L<12>
FSB_D_L<13>
FSB_D_L<14>
FSB_D_L<15>
FSB_DSTB_L_N<0>
FSB_DSTB_L_P<0>
FSB_DINV_L<0>
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FSB_DSTB_L_P<2>
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FSB_D_L<49>
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FSB_D_L<59>
FSB_D_L<60>
FSB_D_L<61>
FSB_D_L<62>
FSB_D_L<63>
FSB_DSTB_L_N<3>
FSB_DSTB_L_P<3>
FSB_DINV_L<3>
CPU_GTLREF
CPU_TEST1
CPU_TEST2
TP_CPU_TEST3
CPU_TEST4
TP_CPU_TEST5
TP_CPU_TEST6
TP_CPU_TEST7
CPU_BSEL<0>
CPU_BSEL<1>
CPU_BSEL<2>
CPU_COMP<0>
CPU_COMP<1>
CPU_COMP<2>
CPU_COMP<3>
CPU_DPRSTP_L
CPU_DPSLP_L
FSB_DPWR_L
CPU_PWRGD
FSB_CPUSLP_L
CPU_PSI_L
R1023 54.9 1% 1/16W MF-LF 402
R1021 54.9 1% 1/16W MF-LF 402
R1022 27.4 1% 1/16W MF-LF 402
R1020 27.4 1% 1/16W MF-LF 402
PLACEMENT_NOTE (all 4 resistors):
Place within 12.7mm of CPU
CPU FSB
SYNC_MASTER=K50
SYNC_DATE=10/30/2008
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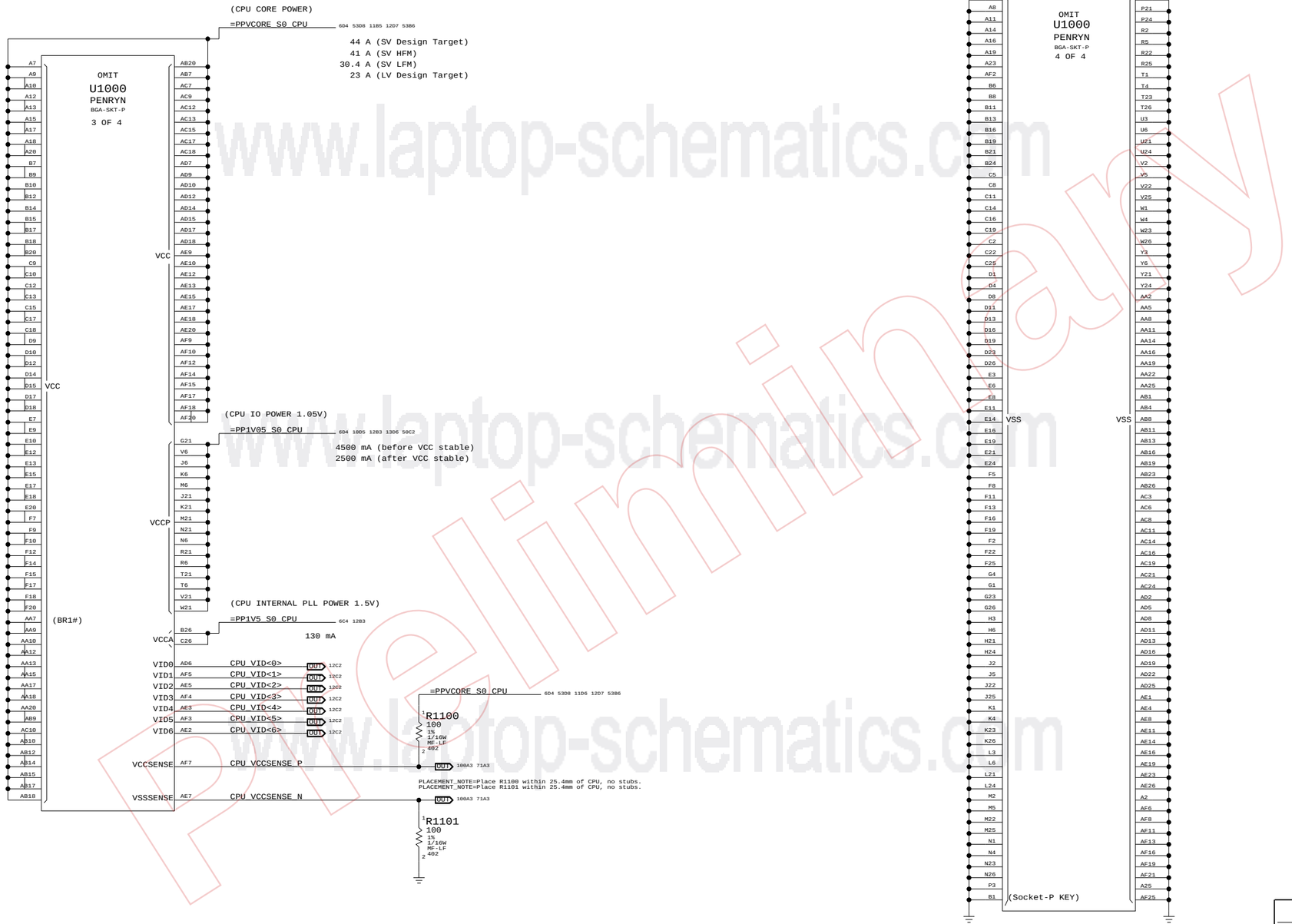
SIZE D
DRAWING NUMBER 051-7840
REV. 10
SCALE NONE
SHT 10 OF 109



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Current numbers from Merom for Santa Rosa EMTS, doc #20905.

CPU Power & Ground

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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SCALE: NONE	SHT 11 OF 109	

CPU VCORE HF AND BULK DECOUPLING

6X 220UF. 32X 22UF 0805

53B6 11D6 11B5 53D8 6D4 =PPVCORE_S0_CPU

NOTE: CHANGED TO X5R CAPS TO MATCH PREVIOUS IMACS AND FOR C4

LAYOUT NOTE:
PLACE INSIDE SOCKET CAVITY (ON BOTTOMSIDE)

NOSTUFF C1200 22UF 20% 6.3V CERM-X5R 805
C1201 22UF 20% 6.3V CERM-X5R 805
C1202 22UF 20% 6.3V CERM-X5R 805
C1203 22UF 20% 6.3V CERM-X5R 805
C1204 22UF 20% 6.3V CERM-X5R 805
C1205 22UF 20% 6.3V CERM-X5R 805
C1206 22UF 20% 6.3V CERM-X5R 805
C1207 22UF 20% 6.3V CERM-X5R 805
C1208 22UF 20% 6.3V CERM-X5R 805
C1209 22UF 20% 6.3V CERM-X5R 805

LAYOUT NOTE:
PLACE INSIDE SOCKET CAVITY (ON BOTTOMSIDE)

C1210 22UF 20% 6.3V CERM-X5R 805
C1211 22UF 20% 6.3V CERM-X5R 805
C1212 22UF 20% 6.3V CERM-X5R 805
C1213 22UF 20% 6.3V CERM-X5R 805
C1214 22UF 20% 6.3V CERM-X5R 805
C1215 22UF 20% 6.3V CERM-X5R 805
C1216 22UF 20% 6.3V CERM-X5R 805
C1217 22UF 20% 6.3V CERM-X5R 805
C1218 22UF 20% 6.3V CERM-X5R 805
C1219 22UF 20% 6.3V CERM-X5R 805

LAYOUT NOTE:
PLACE NEAR SOCKET NORTH SIDE (ON TOPSIDE)

C1220 22UF 20% 6.3V CERM-X5R 805
C1221 22UF 20% 6.3V CERM-X5R 805
NOSTUFF C1222 22UF 20% 6.3V CERM-X5R 805
NOSTUFF C1223 22UF 20% 6.3V CERM-X5R 805
NOSTUFF C1224 22UF 20% 6.3V CERM-X5R 805
NOSTUFF C1225 22UF 20% 6.3V CERM-X5R 805

LAYOUT NOTE:
PLACE NEAR SOCKET SOUTH SIDE (ON TOPSIDE)

C1226 22UF 20% 6.3V CERM-X5R 805
C1227 22UF 20% 6.3V CERM-X5R 805
NOSTUFF C1228 22UF 20% 6.3V CERM-X5R 805
NOSTUFF C1229 22UF 20% 6.3V CERM-X5R 805
C1230 22UF 20% 6.3V CERM-X5R 805
NOSTUFF C1231 22UF 20% 6.3V CERM-X5R 805

LAYOUT NOTE:
PLACE ON BOTTOMSIDE

CRITICAL NOSTUFF C1250 220UF-0.007OHM 20% 2V POLY CASE-D2-SM
CRITICAL C1251 220UF-0.007OHM 20% 2V POLY CASE-D2-SM
CRITICAL C1254 220UF-0.007OHM 20% 2V POLY CASE-D2-SM
CRITICAL C1255 220UF-0.007OHM 20% 2V POLY CASE-D2-SM
CRITICAL C1252 220UF-0.007OHM 20% 2V POLY CASE-D2-SM
CRITICAL C1253 220UF-0.007OHM 20% 2V POLY CASE-D2-SM

LAYOUT NOTE:
PLACE ON BOTTOMSIDE

LAYOUT NOTE:
PLACE NEAR MCP

C1260 0.1UF 20% 10V CERM 402
C1261 0.1UF 20% 10V CERM 402
C1262 0.1UF 20% 10V CERM 402
C1263 0.1UF 20% 10V CERM 402
C1264 0.1UF 20% 10V CERM 402
C1265 0.1UF 20% 10V CERM 402

CPU VCORE VID CONNECTIONS

11B6 CPU_VID<0> = IMVP6_VID<0> MAKE_BASE=TRUE 100A3 71C7
11B6 CPU_VID<1> = IMVP6_VID<1> MAKE_BASE=TRUE 100A3 71C7
11B6 CPU_VID<2> = IMVP6_VID<2> MAKE_BASE=TRUE 100A3 71C7
11B6 CPU_VID<3> = IMVP6_VID<3> MAKE_BASE=TRUE 100A3 71C7
11B6 CPU_VID<4> = IMVP6_VID<4> MAKE_BASE=TRUE 100A3 71C7
11B6 CPU_VID<5> = IMVP6_VID<5> MAKE_BASE=TRUE 100A3 71C7
11B6 CPU_VID<6> = IMVP6_VID<6> MAKE_BASE=TRUE 100A3 71C7

VCCA (CPU AVdd) DECOUPLING

11B6 6C4 =PP1V5_S0_CPU

1x 10uF, 1x 0.01uF

C1280 10uF 20% 6.3V X5R 603
C1281 0.01UF 10% 16V CERM 402

LAYOUT NOTE:
PLACE C1281 NEAR PIN B26 OF U1000

VCCP (CPU I/O) DECOUPLING

50C2 13D6 11C6 10D5 6D4 =PP1V05_S0_CPU

1X 330UF, 6X 0.1UF 0402

CRITICAL C1235 330UF 20% 6.3V ELEC 6.3X8-SM-HF
C1236 0.1UF 20% 10V CERM 402
C1237 0.1UF 20% 10V CERM 402
C1238 0.1UF 20% 10V CERM 402
C1239 0.1UF 20% 10V CERM 402
C1240 0.1UF 20% 10V CERM 402
C1241 0.1UF 20% 10V CERM 402

LAYOUT NOTE:
PLACE C1235 CLOSE TO CPU

CPU Decoupling & VID

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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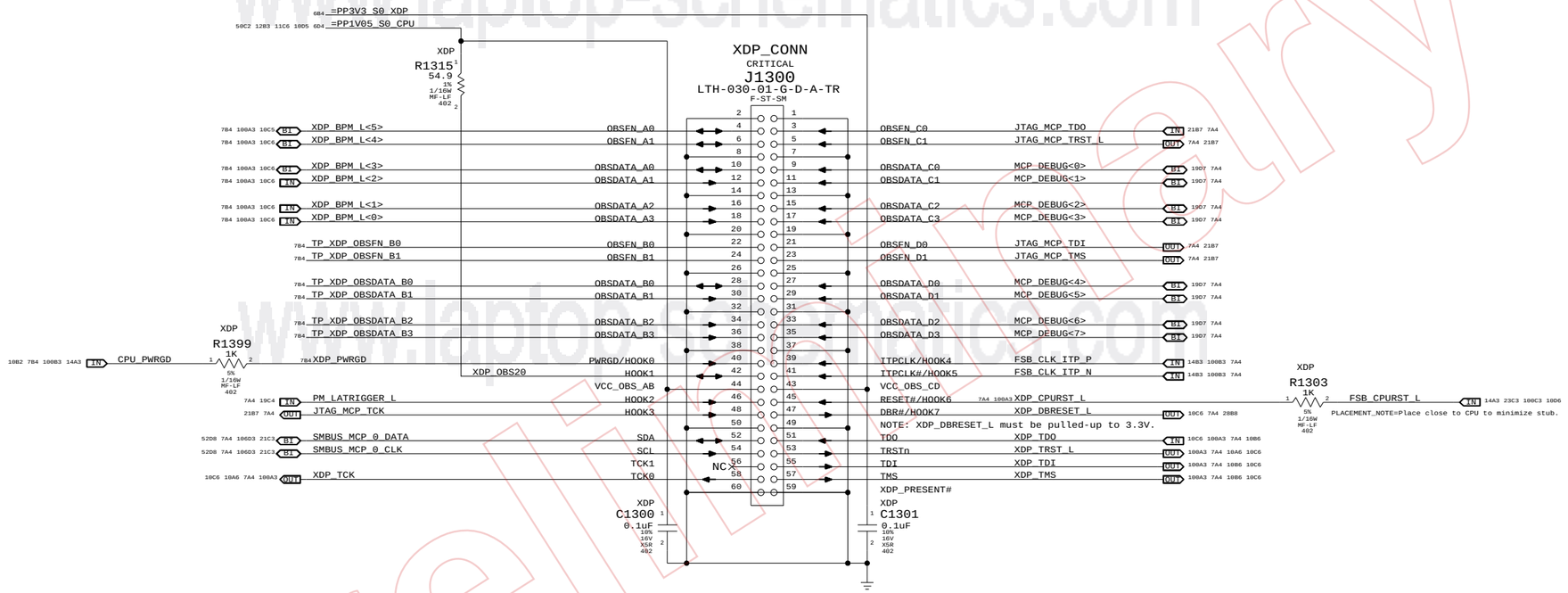
MCP79-specific pinout



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eXtended Debug Port (XDP)

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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OMIT

U1400
MCP79-TOPO-B
BGA
(1 OF 11)

FSB

100D3 10C4 7D8 7D7	BI	FSB_DSTB_L_P<0>	T40	CPU_DSTBP0#	Y43	CPU_D0#	FSB_D_L<0>	BI	7D7 7D8 10C4 100D3
100D3 10C4	BI	FSB_DSTB_L_N<0>	U40	CPU_DSTBN0#	W42	CPU_D1#	FSB_D_L<1>	BI	10C4 100D3
100D3 10C4 7D8 7D7	BI	FSB_DINV_L<0>	V41	CPU_DBI0#	Y40	CPU_D2#	FSB_D_L<2>	BI	10C4 100D3
100D3 10B4 7D8 7D7	BI	FSB_DSTB_L_P<1>	W39	CPU_DSTBP1#	W41	CPU_D3#	FSB_D_L<3>	BI	10C4 100D3
100D3 10B4	BI	FSB_DSTB_L_N<1>	W37	CPU_DSTBN1#	Y39	CPU_D4#	FSB_D_L<4>	BI	10C4 100D3
100D3 10B4	BI	FSB_DINV_L<1>	V35	CPU_DBI1#	V42	CPU_D5#	FSB_D_L<5>	BI	10C4 100D3
100D3 10C2	BI	FSB_DSTB_L_P<2>	N37	CPU_DSTBP2#	Y41	CPU_D6#	FSB_D_L<6>	BI	10C4 100D3
100D3 10C2 7D8 7D7	BI	FSB_DSTB_L_N<2>	L36	CPU_DSTBN2#	Y42	CPU_D7#	FSB_D_L<7>	BI	10C4 100D3
100D3 10C2 7D8 7D7	BI	FSB_DINV_L<2>	N35	CPU_DBI2#	P42	CPU_D8#	FSB_D_L<8>	BI	10C4 100D3
100D3 10B2	BI	FSB_DSTB_L_P<3>	M39	CPU_DSTBP3#	U41	CPU_D9#	FSB_D_L<9>	BI	10C4 100D3
100D3 10B2 7D8 7D7	BI	FSB_DSTB_L_N<3>	M41	CPU_DSTBN3#	R42	CPU_D10#	FSB_D_L<10>	BI	10C4 100D3
100D3 10B2 7D8 7D7	BI	FSB_DINV_L<3>	J41	CPU_DBI3#	T39	CPU_D11#	FSB_D_L<11>	BI	10C4 100D3
					T42	CPU_D12#	FSB_D_L<12>	BI	10C4 100D3
100C3 10D8	BI	FSB_A_L<3>	AC34	CPU_A3#	T41	CPU_D13#	FSB_D_L<13>	BI	10C4 100D3
100C3 10D8	BI	FSB_A_L<4>	AE38	CPU_A4#	R41	CPU_D14#	FSB_D_L<14>	BI	10C4 100D3
100C3 10D8	BI	FSB_A_L<5>	AE34	CPU_A5#	T43	CPU_D15#	FSB_D_L<15>	BI	10C4 100D3
100C3 10D8 7D8 7D7	BI	FSB_A_L<6>	AC37	CPU_A6#	W35	CPU_D16#	FSB_D_L<16>	BI	7D7 7D8 10C4 100D3
100C3 10D8	BI	FSB_A_L<7>	AE37	CPU_A7#	AA37	CPU_D17#	FSB_D_L<17>	BI	10C4 100D3
100C3 10D8	BI	FSB_A_L<8>	AE35	CPU_A8#	W33	CPU_D18#	FSB_D_L<18>	BI	10C4 100D3
100C3 10D8	BI	FSB_A_L<9>	AB35	CPU_A9#	W34	CPU_D19#	FSB_D_L<19>	BI	10C4 100D3
100C3 10D8	BI	FSB_A_L<10>	AF35	CPU_A10#	AA36	CPU_D20#	FSB_D_L<20>	BI	10C4 100D3
100C3 10D8	BI	FSB_A_L<11>	AG35	CPU_A11#	AA34	CPU_D21#	FSB_D_L<21>	BI	10B4 100D3
100C3 10D8	BI	FSB_A_L<12>	AG39	CPU_A12#	AA38	CPU_D22#	FSB_D_L<22>	BI	10B4 100D3
100C3 10D8	BI	FSB_A_L<13>	AE33	CPU_A13#	AA35	CPU_D23#	FSB_D_L<23>	BI	10B4 100D3
100C3 10D8	BI	FSB_A_L<14>	AG37	CPU_A14#	U38	CPU_D24#	FSB_D_L<24>	BI	10B4 100D3
100C3 10D8	BI	FSB_A_L<15>	AG38	CPU_A15#	U36	CPU_D25#	FSB_D_L<25>	BI	10B4 100D3
100C3 10D8	BI	FSB_A_L<16>	AG34	CPU_A16#	U35	CPU_D26#	FSB_D_L<26>	BI	10B4 100D3
100C3 10D8	BI	FSB_A_L<17>	AN38	CPU_A17#	U33	CPU_D27#	FSB_D_L<27>	BI	10B4 100D3
100C3 10C8	BI	FSB_A_L<18>	AL39	CPU_A18#	U34	CPU_D28#	FSB_D_L<28>	BI	10B4 100D3
100C3 10C8	BI	FSB_A_L<19>	AG33	CPU_A19#	W38	CPU_D29#	FSB_D_L<29>	BI	10B4 100D3
100C3 10C8	BI	FSB_A_L<20>	AL33	CPU_A20#	R33	CPU_D30#	FSB_D_L<30>	BI	10B4 100D3
100C3 10C8	BI	FSB_A_L<21>	AJ33	CPU_A21#	U37	CPU_D31#	FSB_D_L<31>	BI	10B4 100D3
100C3 10C8	BI	FSB_A_L<22>	AN36	CPU_A22#	N34	CPU_D32#	FSB_D_L<32>	BI	10C2 100D3
100C3 10C8	BI	FSB_A_L<23>	AJ35	CPU_A23#	N33	CPU_D33#	FSB_D_L<33>	BI	10C2 100D3
100C3 10C8	BI	FSB_A_L<24>	AJ37	CPU_A24#	R34	CPU_D34#	FSB_D_L<34>	BI	10C2 100D3
100C3 10C8	BI	FSB_A_L<25>	AJ36	CPU_A25#	R35	CPU_D35#	FSB_D_L<36>	BI	10C2 100D3
100C3 10C8	BI	FSB_A_L<26>	AJ38	CPU_A26#	P35	CPU_D36#	FSB_D_L<37>	BI	10C2 100D3
100C3 10C8 7D8 7D7	BI	FSB_A_L<27>	AL37	CPU_A27#	R39	CPU_D37#	FSB_D_L<38>	BI	10C2 100D3
100C3 10C8	BI	FSB_A_L<28>	AL34	CPU_A28#	R37	CPU_D38#	FSB_D_L<39>	BI	10C2 100D3
100C3 10C8	BI	FSB_A_L<29>	AN37	CPU_A29#	R38	CPU_D39#	FSB_D_L<40>	BI	10C2 100D3
100C3 10C8	BI	FSB_A_L<30>	AJ34	CPU_A30#	L37	CPU_D40#	FSB_D_L<41>	BI	7D7 7D8 10C2 100D3
100C3 10C8	BI	FSB_A_L<31>	AL38	CPU_A31#	L39	CPU_D41#	FSB_D_L<42>	BI	10C2 100D3
100C3 10C8	BI	FSB_A_L<32>	AL35	CPU_A32#	L38	CPU_D42#	FSB_D_L<43>	BI	10C2 100D3
100C3 10C8	BI	FSB_A_L<33>	AN34	CPU_A33#	M36	CPU_D43#	FSB_D_L<44>	BI	10C2 100D3
100C3 10C8	BI	FSB_A_L<34>	AR39	CPU_A34#	M38	CPU_D44#	FSB_D_L<45>	BI	10C2 100D3
100C3 10C8	BI	FSB_A_L<35>	AN35	CPU_A35#	J39	CPU_D45#	FSB_D_L<46>	BI	10C2 100D3
					J38	CPU_D46#	FSB_D_L<47>	BI	10C2 100D3
100C3 10D8 7D8 7D7	BI	FSB_ADSTB_L<0>	AE36	CPU_ADSTB0#	J37	CPU_D47#	FSB_D_L<48>	BI	10C2 100D3
100C3 10C8 7D8 7D7	BI	FSB_ADSTB_L<1>	AK35	CPU_ADSTB1#	L42	CPU_D48#	FSB_D_L<49>	BI	10C2 100D3
					M42	CPU_D49#	FSB_D_L<50>	BI	10C2 100D3
100C3 10D8 7C8 7C7	BI	FSB_REQ_L<0>	AC38	CPU_REQ0#	P41	CPU_D50#	FSB_D_L<51>	BI	10C2 100D3
100C3 10D8 7C8 7C7	BI	FSB_REQ_L<1>	AA33	CPU_REQ1#	N41	CPU_D51#	FSB_D_L<52>	BI	10C2 100D3
100C3 10D8 7C8 7C7	BI	FSB_REQ_L<2>	AC39	CPU_REQ2#	N40	CPU_D52#	FSB_D_L<53>	BI	10B2 100D3
100C3 10D8 7C8 7C7	BI	FSB_REQ_L<3>	AC33	CPU_REQ3#	M40	CPU_D53#	FSB_D_L<54>	BI	10B2 100D3
100C3 10D8 7C8 7C7	BI	FSB_REQ_L<4>	AC35	CPU_REQ4#	H40	CPU_D54#	FSB_D_L<55>	BI	10B2 100D3
					K42	CPU_D55#	FSB_D_L<56>	BI	10B2 100D3
100C3 10D6	BI	FSB_ADS_L	AD42	CPU_ADS#	H41	CPU_D56#	FSB_D_L<57>	BI	10B2 100D3
100C3 10D6 7D7	BI	FSB_BNR_L	AD43	CPU_BNR#	L41	CPU_D57#	FSB_D_L<58>	BI	10B2 100D3
100C3 23C3 10D6 7D7	BI	FSB_BREQ0_L	AE40	CPU_BR0#	H43	CPU_D58#	FSB_D_L<59>	BI	7D7 7D8 10B2 100D3
100C3		FSB_BREQ1_L	AL32	CPU_BR1#	H42	CPU_D59#	FSB_D_L<60>	BI	10B2 100D3
100C3 10D6 7D7	BI	FSB_DBSY_L	AD39	CPU_DBSY#	K41	CPU_D60#	FSB_D_L<61>	BI	10B2 100D3
100C3 10D6	BI	FSB_DRDY_L	AD41	CPU_DRDY#	J40	CPU_D61#	FSB_D_L<62>	BI	10B2 100D3
100C3 10D6 7D7	BI	FSB_HIT_L	AB42	CPU_HIT#	H39	CPU_D62#	FSB_D_L<63>	BI	10B2 100D3
100C3 10D6 7D7	BI	FSB_HITM_L	AD40	CPU_HITM#	M43	CPU_D63#			
100C3 10D6 7D7	IN	FSB_LOCK_L	AC43	CPU_LOCK#					
10D6 100C3	OUT	FSB_TRDY_L	AE41	CPU_TRDY#	AA41	CPU_BPRI#	FSB_BPRI_L	OUT	10D6 100C3
					AA40	CPU_DEFER#	FSB_DEFER_L	OUT	10D6 100C3
23B5	OUT	CPU_PECI_MCP	E41	CPU_PECI					
100B3 50B3 10C5	OUT	CPU_PROCHOT_L	AJ41	CPU_PROCHOT#	G42	BCLK_OUT_CPU_P	FSB_CLK_CPU_P	OUT	7C8 100B3 10D6
			AG43	CPU_THERMTRIP#	G41	BCLK_OUT_CPU_N	FSB_CLK_CPU_N	OUT	7C8 100B3 7B3 10D6
			AH40	CPU_FERR#	AL43	BCLK_OUT_ITP_P	FSB_CLK_ITP_P	OUT	100B3 7A4 13C3
					AL42	BCLK_OUT_ITP_N	FSB_CLK_ITP_N	OUT	100B3 7A4 13C3
					AL41	BCLK_OUT_NB_P	FSB_CLK_MCP_P	100B3	
					AK42	BCLK_OUT_NB_N	FSB_CLK_MCP_N	100B3	
					AK41	BCLK_IN_N			
					AJ40	BCLK_IN_P			

Loop-back clock for delay matching.

					AF41	CPU_A20M#	CPU_A20M_L	OUT	7D8 100C3 10C8
					AH39	CPU_IGNNE#	CPU_IGNNE_L	OUT	7D8 100B3 10C8
					AH42	CPU_INIT#	CPU_INIT_L	OUT	7D8 100B3 10D6
					AF42	CPU_INTR	CPU_INTR	OUT	7D8 100B3 10C8
					AG41	CPU_NMI	CPU_NMI	OUT	7D8 100B3 10B8
					AH41	CPU_SMI#	CPU_SMI_L	OUT	7C8 100B3 10B8
					AH43	CPU_PWRGD	CPU_PWRGD		
					H38	CPU_RESET#	FSB_CPURST_L	OUT	23C3 100C3 10D6 13C2
					AM33	CPU_SLP#	FSB_CPUSLP_L	OUT	100B3 10B2
					AN33	CPU_DPSLP#	CPU_DPSLP_L	OUT	100B3 10B2
					AM32	CPU_DPWR#	FSB_DPWR_L	OUT	7C7 100B3 10B2
					AG42	CPU_STPCLK#	CPU_STPCLK_L	OUT	7D8 100B3 10C8
					AN32	CPU_DPRSTP#	CPU_DPRSTP_L	OUT	100B3 10B2 71C7

25C8 23C3 22D3 14A2 6D4 =PP1V05_S0_MCP_FSB

R1410 54.9 1% 1/16W MF-LF 402
R1415 62 5% 1/16W MF-LF 402
R1416 62 5% 1/16W MF-LF 402

100B3 50B1 10C6	IN	PM_THRMTRIP_L	
100B3 10C8	IN	CPU_FERR_L	

NO STUFF
R1420 1K 5% 1/16W MF-LF 402
NO STUFF
R1421 1K 5% 1/16W MF-LF 402
NO STUFF
R1422 1K 5% 1/16W MF-LF 402

23B5	IN	=MCP_BSEL<2>	(MCP_BSEL<2>)	F42 CPU_BSEL2
23C5	IN	=MCP_BSEL<1>	(MCP_BSEL<1>)	D42 CPU_BSEL1
23C5	IN	=MCP_BSEL<0>	(MCP_BSEL<0>)	F41 CPU_BSEL0

10D6 100C3	OUT	FSB_RS_L<0>	AC41	CPU_RS0#
10D6 100C3	OUT	FSB_RS_L<1>	AB41	CPU_RS1#
10D6 100C3	OUT	FSB_RS_L<2>	AC42	CPU_RS2#

R1430 49.9 1% 1/16W MF-LF 402
R1435 49.9 1% 1/16W MF-LF 402
R1431 49.9 1% 1/16W MF-LF 402
R1436 49.9 1% 1/16W MF-LF 402

25C2 PP1V05_S0_MCP_PLL_FSB
270 mA (A01)

206 mA	AG27	+V_DLL_DLCELL_AVDD
20 mA	AH27	+V_PLL_MCLK
29 mA	AG28	+V_PLL_FSB
15 mA	AH28	+V_PLL_CPU

100B3	MCP_BCLK_VML_COMP_VDD	AM39	BCLK_VML_COMP_VDD
100B3	MCP_BCLK_VML_COMP_GND	AM40	BCLK_VML_COMP_GND
100B3	MCP_CPU_COMP_VCC	AM43	CPU_COMP_VCC
100B3	MCP_CPU_COMP_GND	AM42	CPU_COMP_GND

=PP1V05_S0_MCP_FSB 6D4 14B7 22D3 23C3 25C8
NO STUFF
R1440 150 5% 1/16W MF-LF 402
OUT 100B3 7B4 10B2 13C7

MCP CPU Interface

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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SIZE	DRAWING NUMBER	REV.
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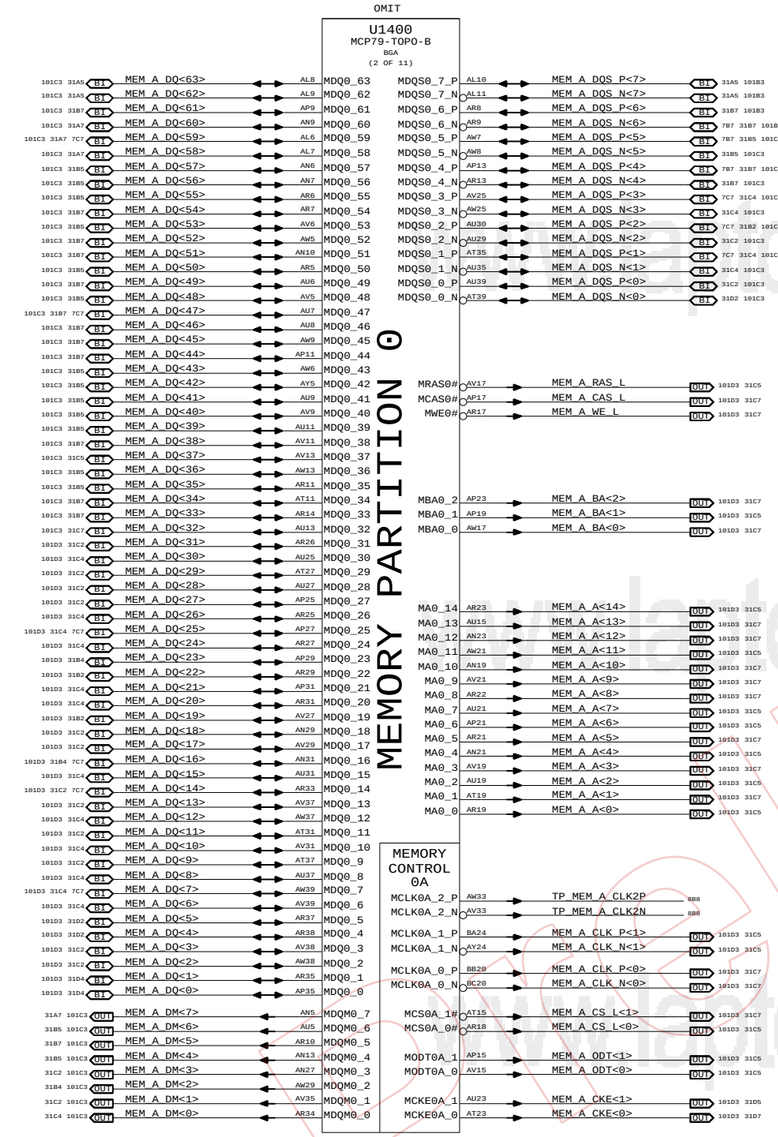
SCALE	SHT	OF
NONE	14	109

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).


OMIT
U1400
MCP79-TOPO-B
BGA
(2 OF 11)
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MCAS0# MEM_A_CAS_L
MWE0# MEM_A_WE_L
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MBA0_1 MEM_A_BA<1>
MBA0_0 MEM_A_BA<0>
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MA0_11 MEM_A_A<11>
MA0_10 MEM_A_A<10>
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OMIT
U1400
MCP79-TOPO-B
BGA
(3 OF 11)
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MEM_B_DQ<9> MDQ1_9
MEM_B_DQ<8> MDQ1_8
MEM_B_DQ<7> MDQ1_7
MEM_B_DQ<6> MDQ1_6
MEM_B_DQ<5> MDQ1_5
MEM_B_DQ<4> MDQ1_4
MEM_B_DQ<3> MDQ1_3
MEM_B_DQ<2> MDQ1_2
MEM_B_DQ<1> MDQ1_1
MEM_B_DQ<0> MDQ1_0
MEM_B_DM<7> MDQM1_7
MEM_B_DM<6> MDQM1_6
MEM_B_DM<5> MDQM1_5
MEM_B_DM<4> MDQM1_4
MEM_B_DM<3> MDQM1_3
MEM_B_DM<2> MDQM1_2
MEM_B_DM<1> MDQM1_1
MEM_B_DM<0> MDQM1_0
MDQS1_7_P MEM_B_DQS_P<7>
MDQS1_7_N MEM_B_DQS_N<7>
MDQS1_6_P MEM_B_DQS_P<6>
MDQS1_6_N MEM_B_DQS_N<6>
MDQS1_5_P MEM_B_DQS_P<5>
MDQS1_5_N MEM_B_DQS_N<5>
MDQS1_4_P MEM_B_DQS_P<4>
MDQS1_4_N MEM_B_DQS_N<4>
MDQS1_3_P MEM_B_DQS_P<3>
MDQS1_3_N MEM_B_DQS_N<3>
MDQS1_2_P MEM_B_DQS_P<2>
MDQS1_2_N MEM_B_DQS_N<2>
MDQS1_1_P MEM_B_DQS_P<1>
MDQS1_1_N MEM_B_DQS_N<1>
MDQS1_0_P MEM_B_DQS_P<0>
MDQS1_0_N MEM_B_DQS_N<0>
MRAS1# MEM_B_RAS_L
MCAS1# MEM_B_CAS_L
MWE1# MEM_B_WE_L
MBA1_2 MEM_B_BA<2>
MBA1_1 MEM_B_BA<1>
MBA1_0 MEM_B_BA<0>
MA1_14 MEM_B_A<14>
MA1_13 MEM_B_A<13>
MA1_12 MEM_B_A<12>
MA1_11 MEM_B_A<11>
MA1_10 MEM_B_A<10>
MA1_9 MEM_B_A<9>
MA1_8 MEM_B_A<8>
MA1_7 MEM_B_A<7>
MA1_6 MEM_B_A<6>
MA1_5 MEM_B_A<5>
MA1_4 MEM_B_A<4>
MA1_3 MEM_B_A<3>
MA1_2 MEM_B_A<2>
MA1_1 MEM_B_A<1>
MA1_0 MEM_B_A<0>
MEMORY CONTROL 1A
MCLK1A_2_P TP_MEM_B_CLK2P
MCLK1A_2_N TP_MEM_B_CLK2N
MCLK1A_1_P MEM_B_CLK_P<1>
MCLK1A_1_N MEM_B_CLK_N<1>
MCLK1A_0_P MEM_B_CLK_P<0>
MCLK1A_0_N MEM_B_CLK_N<0>
MCS1A_1# MEM_B_CS_L<1>
MCS1A_0# MEM_B_CS_L<0>
MODT1A_1 MEM_B_ODT<1>
MODT1A_0 MEM_B_ODT<0>
MCKE1A_1 MEM_B_CKE<1>
MCKE1A_0 MEM_B_CKE<0>
MCP Memory Interface
SYNC_MASTER=K50
SYNC_DATE=10/30/2008
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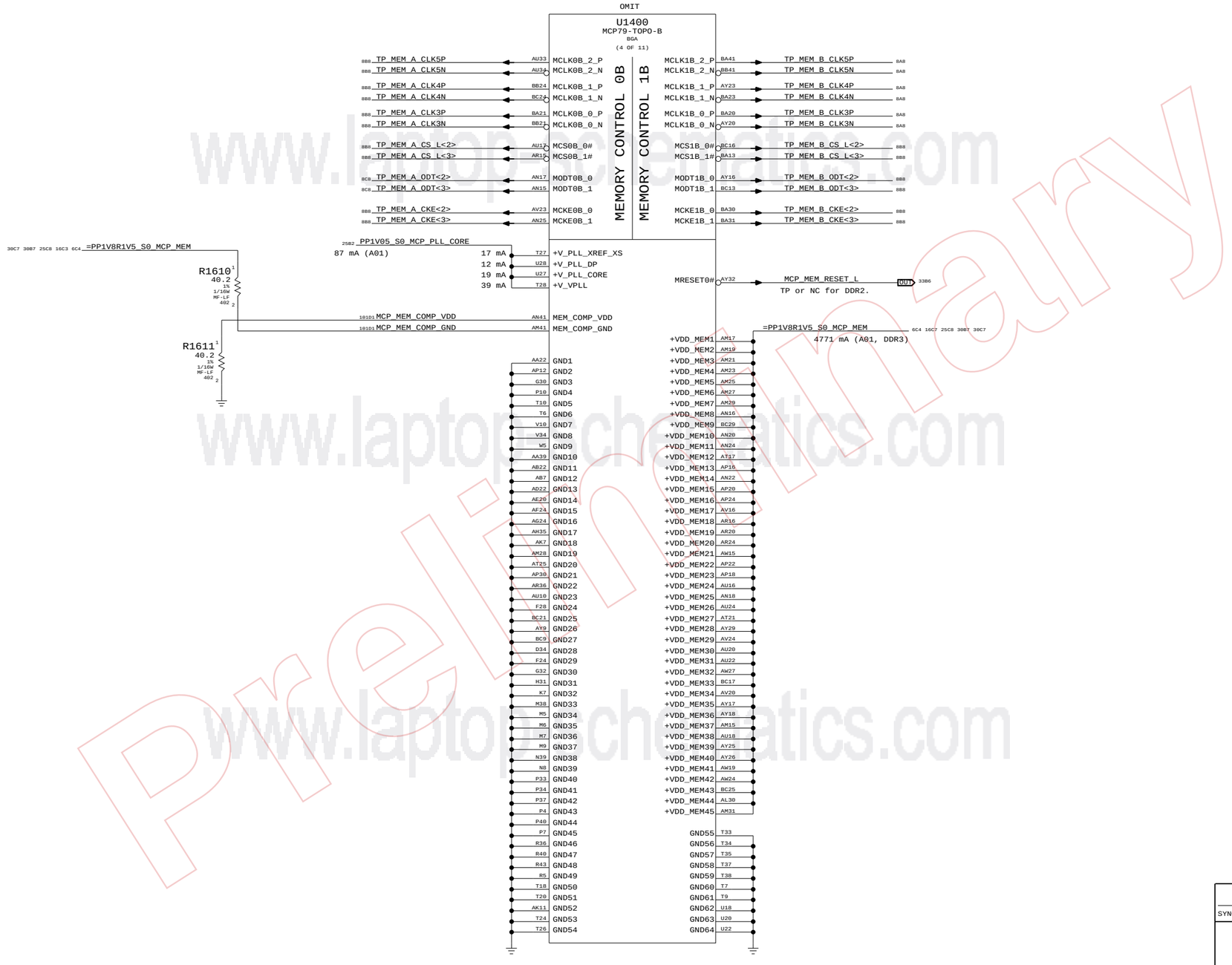
SIZE D
DRAWING NUMBER 051-7840
REV. 10
SCALE NONE
SHT 15 OF 109



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MCP Memory Misc

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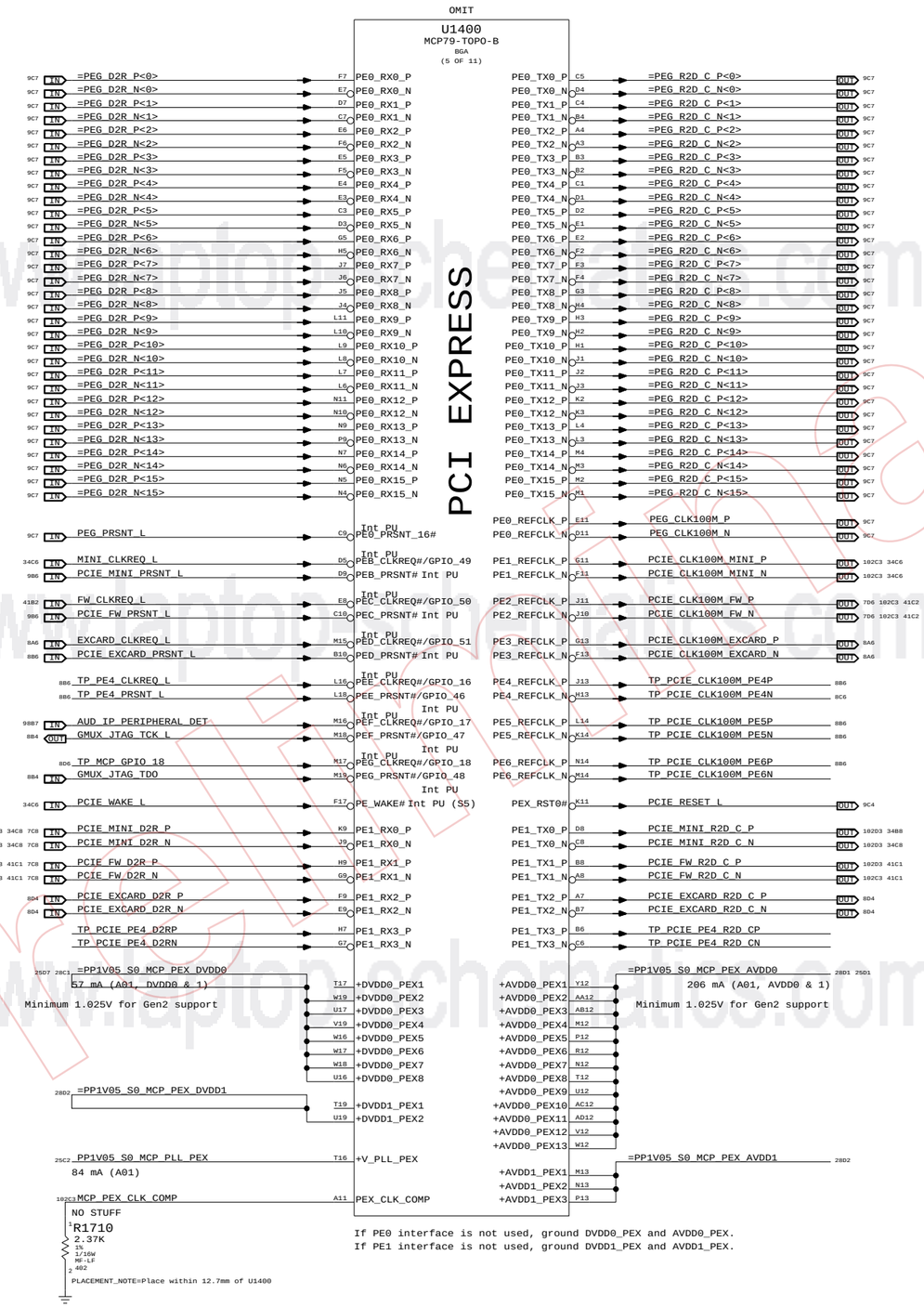

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MCP PCIe Interfaces

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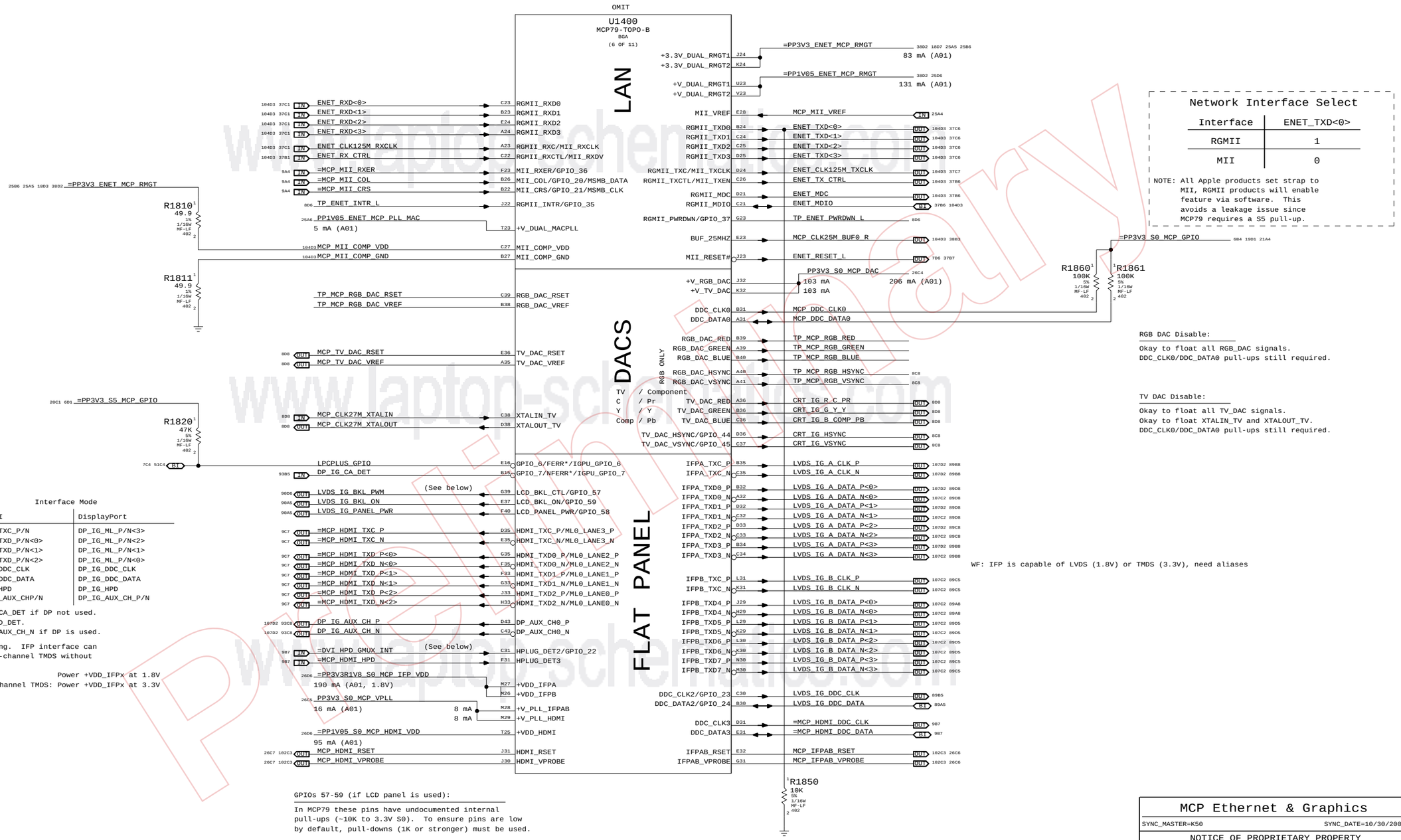
OMIT
U1400
MCP79-TOPO-B
BGA
(6 OF 11)
LAN
DACS
RGB ONLY
TV / Component
C / Pr
Y / Y
Comp / Pb
FLAT PANEL
(See below)
(See below)
ENET_RXD<0>
ENET_RXD<1>
ENET_RXD<2>
ENET_RXD<3>
ENET_CLK125M_RXCLK
ENET_RX_CTRL
=MCP_MII_RXER
=MCP_MII_COL
=MCP_MII_CRS
TP_ENET_INTR_L
PP1V05_ENET_MCP_PLL_MAC
5 mA (A01)
MCP_MII_COMP_VDD
MCP_MII_COMP_GND
TP_MCP_RGB_DAC_RSET
TP_MCP_RGB_DAC_VREF
MCP_TV_DAC_RSET
MCP_TV_DAC_VREF
MCP_CLK27M_XTALIN
MCP_CLK27M_XTALOUT
LPCPLUS_GPIO
DP_IG_CA_DET
LVDS_IG_BKL_PWM
LVDS_IG_BKL_ON
LVDS_IG_PANEL_PWR
=MCP_HDMI_TXC_P
=MCP_HDMI_TXC_N
=MCP_HDMI_TXD_P<0>
=MCP_HDMI_TXD_N<0>
=MCP_HDMI_TXD_P<1>
=MCP_HDMI_TXD_N<1>
=MCP_HDMI_TXD_P<2>
=MCP_HDMI_TXD_N<2>
DP_IG_AUX_CH_P
DP_IG_AUX_CH_N
=DVI_HPD_GMUX_INT
=MCP_HDMI_HPD
=PP3V3R1V8_S0_MCP_IFP_VDD
190 mA (A01, 1.8V)
PP3V3_S0_MCP_VPLL
16 mA (A01)
8 mA
8 mA
=PP1V05_S0_MCP_HDMI_VDD
95 mA (A01)
MCP_HDMI_RSET
MCP_HDMI_VPROBE
RGMII_RXD0
RGMII_RXD1
RGMII_RXD2
RGMII_RXD3
RGMII_RXC/MII_RXCLK
RGMII_RXCTL/MII_RXDV
MII_RXER/GPIO_36
MII_COL/GPIO_20/MSMB_DATA
MII_CRS/GPIO_21/MSMB_CLK
RGMII_INTR/GPIO_35
+V_DUAL_MACPLL
MII_COMP_VDD
MII_COMP_GND
RGB_DAC_RSET
RGB_DAC_VREF
TV_DAC_RSET
TV_DAC_VREF
XTALIN_TV
XTALOUT_TV
GPIO_6/FERR*/IGPU_GPIO_6
GPIO_7/NFERR*/IGPU_GPIO_7
LCD_BKL_CTL/GPIO_57
LCD_BKL_ON/GPIO_59
LCD_PANEL_PWR/GPIO_58
HDMI_TXC_P/ML0_LANE3_P
HDMI_TXC_N/ML0_LANE3_N
HDMI_TXD0_P/ML0_LANE2_P
HDMI_TXD0_N/ML0_LANE2_N
HDMI_TXD1_P/ML0_LANE1_P
HDMI_TXD1_N/ML0_LANE1_N
HDMI_TXD2_P/ML0_LANE0_P
HDMI_TXD2_N/ML0_LANE0_N
DP_AUX_CH0_P
DP_AUX_CH0_N
HPLUG_DET2/GPIO_22
HPLUG_DET3
+VDD_IFPA
+VDD_IFPB
+V_PLL_IFPAB
+V_PLL_HDMI
+VDD_HDMI
HDMI_RSET
HDMI_VPROBE
=PP3V3_ENET_MCP_RMGT
83 mA (A01)
=PP1V05_ENET_MCP_RMGT
131 mA (A01)
MCP_MII_VREF
ENET_TXD<0>
ENET_TXD<1>
ENET_TXD<2>
ENET_TXD<3>
ENET_CLK125M_TXCLK
ENET_TX_CTRL
ENET_MDC
ENET_MDIO
TP_ENET_PWRDWN_L
MCP_CLK25M_BUF0_R
ENET_RESET_L
PP3V3_S0_MCP_DAC
103 mA
103 mA
206 mA (A01)
MCP_DDC_CLK0
MCP_DDC_DATA0
TP_MCP_RGB_RED
TP_MCP_RGB_GREEN
TP_MCP_RGB_BLUE
TP_MCP_RGB_HSYNC
TP_MCP_RGB_VSYNC
CRT_IG_R_C_PR
CRT_IG_G_Y_Y
CRT_IG_B_COMP_PB
CRT_IG_HSYNC
CRT_IG_VSYNC
LVDS_IG_A_CLK_P
LVDS_IG_A_CLK_N
LVDS_IG_A_DATA_P<0>
LVDS_IG_A_DATA_N<0>
LVDS_IG_A_DATA_P<1>
LVDS_IG_A_DATA_N<1>
LVDS_IG_A_DATA_P<2>
LVDS_IG_A_DATA_N<2>
LVDS_IG_A_DATA_P<3>
LVDS_IG_A_DATA_N<3>
LVDS_IG_B_CLK_P
LVDS_IG_B_CLK_N
LVDS_IG_B_DATA_P<0>
LVDS_IG_B_DATA_N<0>
LVDS_IG_B_DATA_P<1>
LVDS_IG_B_DATA_N<1>
LVDS_IG_B_DATA_P<2>
LVDS_IG_B_DATA_N<2>
LVDS_IG_B_DATA_P<3>
LVDS_IG_B_DATA_N<3>
LVDS_IG_DDC_CLK
LVDS_IG_DDC_DATA
=MCP_HDMI_DDC_CLK
=MCP_HDMI_DDC_DATA
MCP_IFPAB_RSET
MCP_IFPAB_VPROBE
R1850
10K
R1860
100K
R1861
100K
=PP3V3_S0_MCP_GPIO
=PP3V3_S5_MCP_GPIO
R1810
49.9
R1811
49.9
R1820
47K
Network Interface Select
Interface
ENET_TXD<0>
RGMII
1
MII
0
NOTE: All Apple products set strap to MII, RGMII products will enable feature via software. This avoids a leakage issue since MCP79 requires a S5 pull-up.
RGB DAC Disable:
Okay to float all RGB_DAC signals.
DDC_CLK0/DDC_DATA0 pull-ups still required.
TV DAC Disable:
Okay to float all TV_DAC signals.
Okay to float XTALIN_TV and XTALOUT_TV.
DDC_CLK0/DDC_DATA0 pull-ups still required.
WF: IFP is capable of LVDS (1.8V) or TMDS (3.3V), need aliases
Interface Mode
MCP Signal | TMDS/HDMI | DisplayPort
=MCP_HDMI_TXC_P/N | TMDS_IG_TXC_P/N | DP_IG_ML_P/N<3>
=MCP_HDMI_TXD_P/N<0> | TMDS_IG_TXD_P/N<0> | DP_IG_ML_P/N<2>
=MCP_HDMI_TXD_P/N<1> | TMDS_IG_TXD_P/N<1> | DP_IG_ML_P/N<1>
=MCP_HDMI_TXD_P/N<2> | TMDS_IG_TXD_P/N<2> | DP_IG_ML_P/N<0>
=MCP_HDMI_DDC_CLK | TMDS_IG_DDC_CLK | DP_IG_DDC_CLK
=MCP_HDMI_DDC_DATA | TMDS_IG_DDC_DATA | DP_IG_DDC_DATA
=MCP_HDMI_HPD | TMDS_IG_HPD | DP_IG_HPD
DP_IG_AUX_CH_P/N | TP_DP_IG_AUX_CHP/N | DP_IG_AUX_CH_P/N
NOTE: 1M pull-down required on DP_IG_CA_DET if DP not used.
NOTE: 20K pull-down required on DP_HPD_DET.
NOTE: 1K pull-down required on DP_IG_AUX_CH_N if DP is used.
NOTE: HDMI port requires level-shifting. IFP interface can be used to provide HDMI or dual-channel TMDS without level-shifters.
LVDS: Power +VDD_IFPx at 1.8V
Dual-channel TMDS: Power +VDD_IFPx at 3.3V
GPIOs 57-59 (if LCD panel is used):
In MCP79 these pins have undocumented internal pull-ups (~10K to 3.3V S0). To ensure pins are low by default, pull-downs (1K or stronger) must be used.
=DVI_HPD_GMUX_INT:
Alias to DVI_HPD for systems using IFP for DVI.
Alias to GMUX_INT for systems with GMUX.
Alias to HPLUG_DET2 for other systems.
Pull-down (20k) required in all cases.
MCP Ethernet & Graphics
SYNC_MASTER=K50
SYNC_DATE=10/30/2008
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REV. 10
SCALE NONE
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OMIT

U1400
MCP79-TOPO-B
BGA
(7 OF 11)

PCI

19D2 7B3 103D3	PCI_REQ0_L	T2	PCI_REQ0#	R3	PCI_GNT0#	TP_PCI_GNT0_L 8C6
19D2 7B3 103D3	PCI_REQ1_L	V9	PCI_REQ1#/FANRPM2	U10	PCI_GNT1#/FANCTL2	TP_PCI_GNT1_L 8C6
19D2 OUT	CRTMUX_SEL_TV_L	T3	PCI_REQ2#/GPIO_40/RS232_DSR#	R4	PCI_GNT2#/GPIO_41/RS232_DTR#	GMUX_JTAG_TMS OUT 8B4
98C7 OUT	AUD_IPHS_SWITCH_EN	U9	PCI_REQ3#/GPIO_38/RS232_CTS#	U11	PCI_GNT3#/GPIO_39/RS232_RTS#	GMUX_JTAG_TDI OUT 8B4
19D2 IN	MCP_RS232_SIN_L	T4	PCI_REQ4#/GPIO_52/RS232_SIN#	P3	PCI_GNT4#/GPIO_53/RS232_SOUT#	MCP_RS232_SOUT_L OUT 19D2
7A4 13C3 BI	MCP_DEBUG<0>	AC3	PCI_AD0	AA3	PCI_CBE0#	TP_PCI_C_BE_L<0> 8C8
7A4 13C3 BI	MCP_DEBUG<1>	AE10	PCI_AD1	AA6	PCI_CBE1#	TP_PCI_C_BE_L<1> 8C8
7A4 13C3 BI	MCP_DEBUG<2>	AC4	PCI_AD2	AA11	PCI_CBE2#	TP_PCI_C_BE_L<2>
7A4 13C3 BI	MCP_DEBUG<3>	AE11	PCI_AD3	W10	PCI_CBE3#	TP_PCI_C_BE_L<3> 8D6
7A4 13C3 BI	MCP_DEBUG<4>	AB3	PCI_AD4	AA9	PCI_DEVSEL#	TP_PCI_DEVSEL_L 8C8
7A4 13C3 BI	MCP_DEBUG<5>	AC6	PCI_AD5	Y4	PCI_FRAME#	TP_PCI_FRAME_L 8C6
7A4 13C3 BI	MCP_DEBUG<6>	AB2	PCI_AD6	AA10	PCI_IRDY#	TP_PCI_IRDY_L 8C8
7A4 13C3 BI	MCP_DEBUG<7>	AC7	PCI_AD7	Y1	PCI_PAR	TP_PCI_PAR 8C6
8A6	TP_PCI_AD<8>	AC8	PCI_AD8	AB9	PCI_PERR#/GPIO_43/RS232_DCD#	TP_PCI_PERR_L 8C8
	TP_PCI_AD<9>	AA2	PCI_AD9	AA7	PCI_SERR#	TP_PCI_SERR_L 8C8
8A6	TP_PCI_AD<10>	AC9	PCI_AD10	Y2	PCI_STOP#	TP_PCI_STOP_L 8C6
8A6	TP_PCI_AD<11>	AC10	PCI_AD11	T1	PCI_PME#/GPIO_30 Int PU (S5)	PM_LATRIGGER_L OUT 7A4 13C6
8A6	TP_PCI_AD<12>	AC11	PCI_AD12	R10	PCI_RESET0#	MEM_VTT_EN_R OUT 9C4
	TP_PCI_AD<13>	AA1	PCI_AD13	R11	PCI_RESET1#	TP_PCI_RESET1_L 8C6
	TP_PCI_AD<14>	AA5	PCI_AD14	R6	PCI_CLK0	TP_PCI_CLK0 8D6
8C6	TP_PCI_AD<15>	Y5	PCI_AD15	R7	PCI_CLK1	TP_PCI_CLK1 8C6
8C6	TP_PCI_AD<16>	W3	PCI_AD16	R8	PCI_CLK2	PCI_CLK33M_MCP_R 103D3
8C6	TP_PCI_AD<17>	W6	PCI_AD17	R9	PCI_CLKIN	PCI_CLK33M_MCP 103D3
8C6	TP_PCI_AD<18>	W4	PCI_AD18			
8C6	TP_PCI_AD<19>	W7	PCI_AD19			
8C6	TP_PCI_AD<20>	V3	PCI_AD20			
8C6	TP_PCI_AD<21>	W8	PCI_AD21			
8C6	TP_PCI_AD<22>	V2	PCI_AD22			
8C6	TP_PCI_AD<23>	W9	PCI_AD23			
8C6	TP_PCI_AD<24>	U3	PCI_AD24			
8C6	TP_PCI_AD<25>	W11	PCI_AD25			
8C6	TP_PCI_AD<26>	U2	PCI_AD26			
8C6	TP_PCI_AD<27>	U5	PCI_AD27			
8C6	TP_PCI_AD<28>	U1	PCI_AD28			
8C6	TP_PCI_AD<29>	U6	PCI_AD29			
8C6	TP_PCI_AD<30>	T5	PCI_AD30			
8C6	TP_PCI_AD<31>	U7	PCI_AD31			

R1910
22
5% 1/16W MF-LF 402
PLACEMENT_NOTE=Place close to pin R8

LPC

8C6	TP_PCI_INTW_L	P2	PCI_INTW#	AD4	LPC_FRAME#	LPC_FRAME_R_L R1960 22 5% 1/16W MF-LF 402 LPC_FRAME_L OUT 103D3 7D4 49C8 51D5
8C6	TP_PCI_INTX_L	N3	PCI_INTX#	AE12	LPC_PWRDWN#/GPIO_54/EXT_NMI#	LPC_PWRDWN_L OUT 7C4 49C5 51D4
8C6	TP_PCI_INTY_L	N2	PCI_INTY#	AE5	LPC_RESET0#	LPC_RESET_L OUT 103D3 9D4
8C6	TP_PCI_INTZ_L	N1	PCI_INTZ#	AD3 103D3	LPC_AD0	LPC_AD_R<0> R1950 22 5% 1/16W MF-LF 402 LPC_AD<0> BI 49C8 51D5 103D3 7D4
8C6	TP_PCI_TRDY_L	Y3	PCI_TRDY#	AD2 103D3	LPC_AD1	LPC_AD_R<1> R1951 22 5% 1/16W MF-LF 402 LPC_AD<1> BI 78B 7D6 49C8 51D5 103D3 7D4
7D4 51D5 49C5 7C8 IN	PM_CLKRUN_L	AD11	PCI_CLKRUN#/GPIO_42	AD1 103D3	LPC_AD2	LPC_AD_R<2> R1952 22 5% 1/16W MF-LF 402 LPC_AD<2> BI 49C8 51D4 103D3 7D4
41B2 IN	FW_PME_L	AE2	LPC_DRQ1#/GPIO_19 Int PU	AD5 103D3	LPC_AD3	LPC_AD_R<3> R1953 22 5% 1/16W MF-LF 402 LPC_AD<3> BI 49C8 51D4 103D3 7D4
8C6	TP_LPC_DRQ0_L	AE1	LPC_DRQ0# Int PU			
7D4 51D4 49C8 BI	LPC_SERIRQ	AE6	LPC_SERIRQ Int PU	AE9	LPC_CLK0	LPC_CLK33M_SMC_R OUT 103D3 9B4

R1961
10K
5% 1/16W MF-LF 402
Strap for Boot ROM Selection (See HDA_SDOUT)

GND

U24	GND65	GND98	Y26
U26	GND66	GND99	Y27
U39	GND67	GND100	AB18
U4	GND68	GND101	H34
U8	GND69	GND102	AB20
V16	GND70	GND103	AB21
V17	GND71	GND104	AB23
V18	GND72	GND105	AB24
V20	GND73	GND106	AB25
V22	GND74	GND107	AB26
V24	GND75	GND108	AB27
V26	GND76	GND109	AB28
V27	GND77	GND110	AB34
V28	GND78	GND111	AB37
V33	GND79	GND112	AB4
V37	GND80	GND113	AB40
V4	GND81	GND114	AC22
V40	GND82	GND115	AC36
V7	GND83	GND116	AC40
W20	GND84	GND117	AB33
W22	GND85	GND118	AC5
W24	GND86	GND119	AD16
W36	GND87	GND120	AD17
W40	GND88	GND121	AD18
W43	GND89	GND122	AD19
Y16	GND90	GND123	AD20
Y17	GND91	GND124	AD24
Y18	GND92	GND125	AD25
Y19	GND93	GND126	AD26
Y20	GND94	GND127	AD27
Y22	GND95	GND128	AD28
Y24	GND96	GND129	AD33
Y25	GND97	GND130	AD34

21A4 18C1 6B4 =PP3V3_S0_MCP_GPIO

19D4	MCP_RS232_SOUT_L	R1989	8.2K	5% 1/16W MF-LF 402		
19D7 7B3 103D3	PCI_REQ0_L	R1990	8.2K	5% 1/16W MF-LF 402		
19D7 7B3 103D3	PCI_REQ1_L	R1991	8.2K	5% 1/16W MF-LF 402		
19D7	CRTMUX_SEL_TV_L	R1992	8.2K	5% 1/16W MF-LF 402		
19D7	MCP_RS232_SIN_L	R1994	8.2K	5% 1/16W MF-LF 402		

MCP PCI & LPC

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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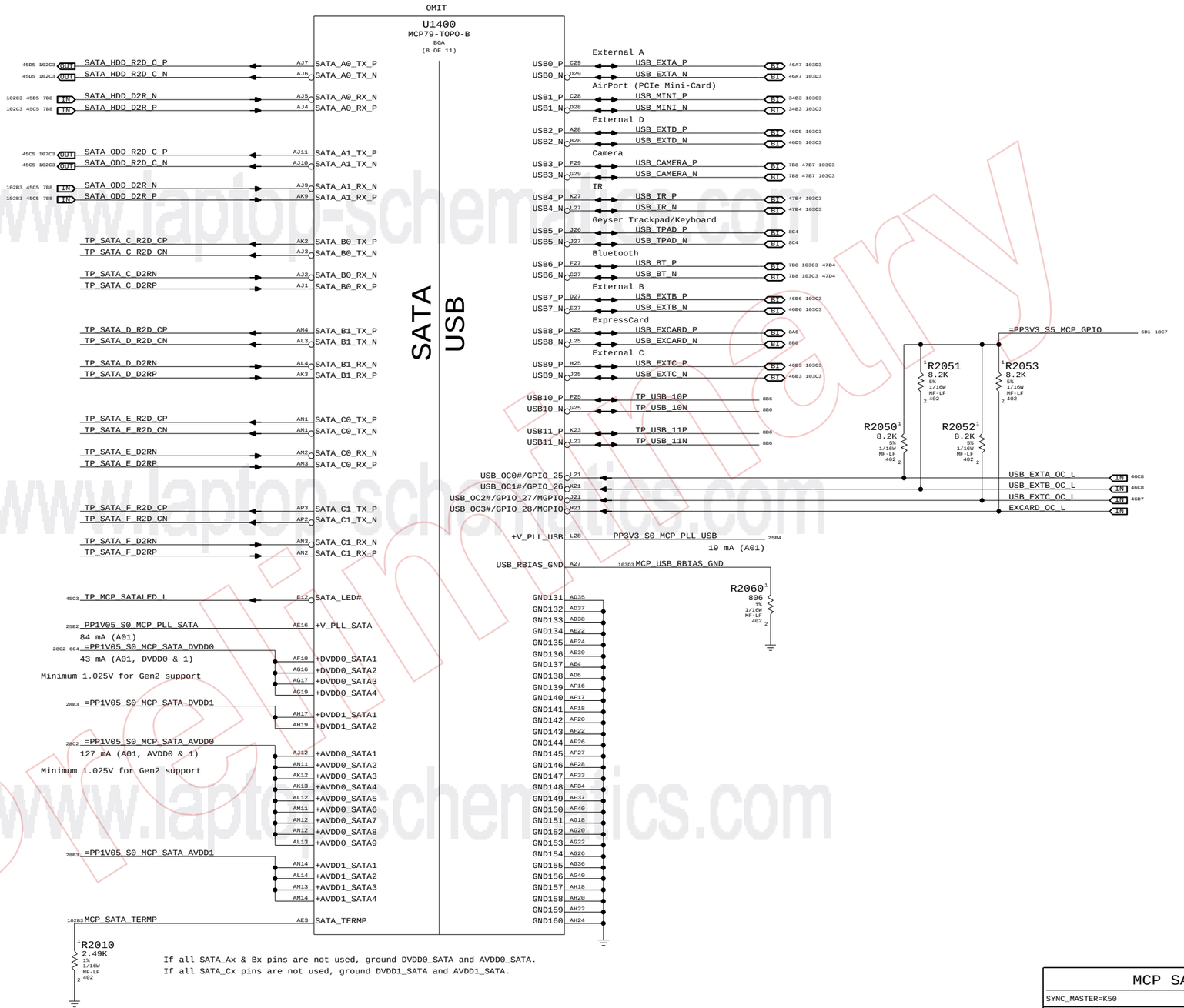

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MCP SATA & USB

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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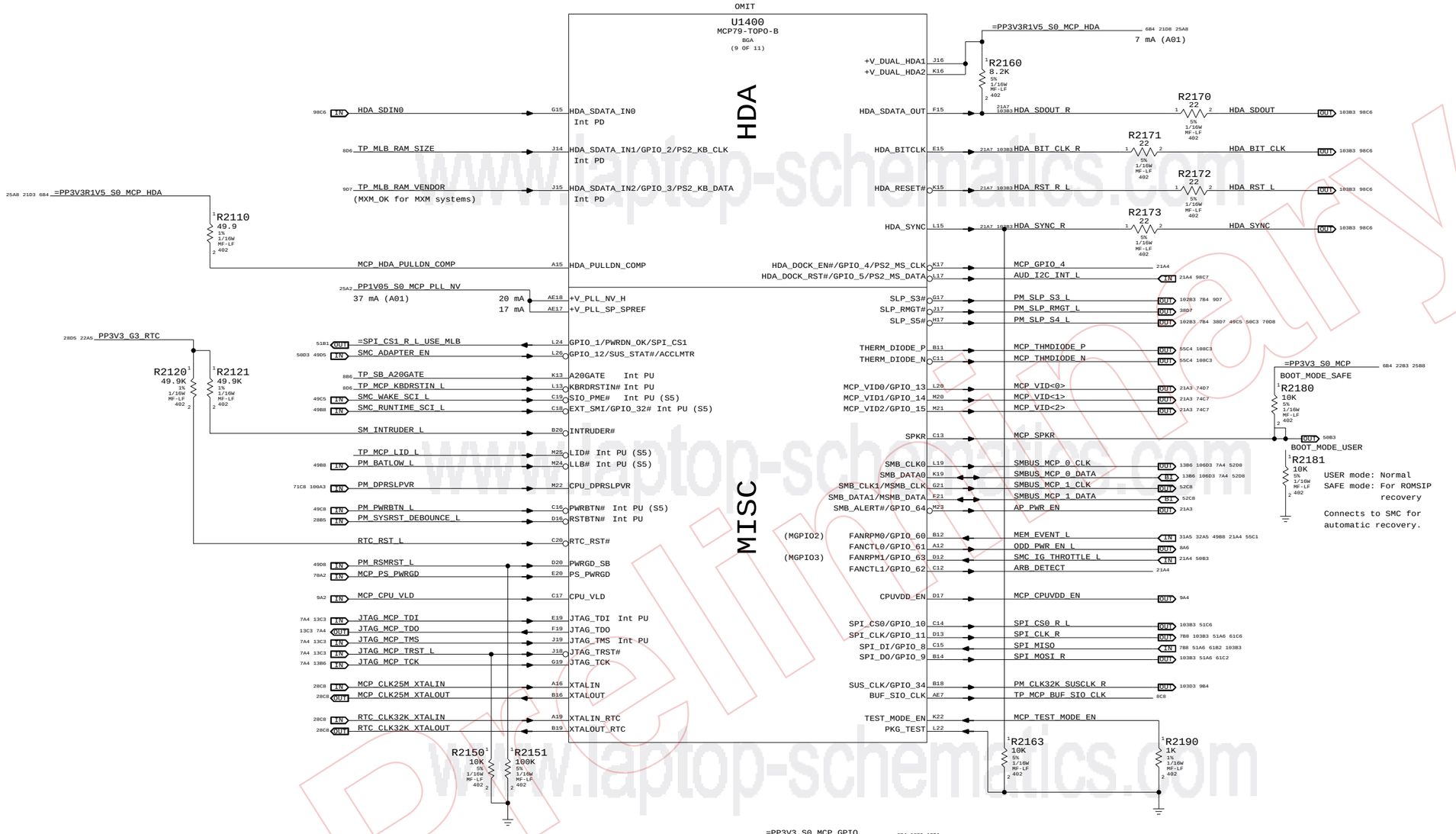
SIZE	DRAWING NUMBER	REV.
D	051-7840	10

SCALE	SHT	OF
NONE	20	109

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).



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OMIT

U1400
MCP79-TOPO-B
BGA
(11 OF 11)

GND

AH26	GND161	GND253	AV40
AH33	GND162	GND254	BA1
AH34	GND163	GND255	BA4
AH37	GND164	GND256	AW31
AH38	GND165	GND257	AY6
AJ39	GND166	GND258	L35
AJ8	GND167	GND259	BC33
AK10	GND168	GND260	BC37
AK33	GND169	GND261	BC41
AK34	GND170	GND262	AY14
AK37	GND171	GND263	BC5
AK4	GND172	GND264	C2
AK40	GND173	GND265	D10
AL36	GND174	GND266	D14
AL40	GND175	GND267	D15
AL5	GND176	GND268	D18
AM10	GND177	GND269	D19
AM16	GND178	GND270	D22
AM18	GND179	GND271	D23
AM20	GND180	GND272	D26
AM22	GND181	GND273	D30
AM24	GND182	GND274	D37
AM26	GND183	GND275	D6
AM30	GND184	GND276	E13
AM34	GND185	GND277	E17
AM35	GND186	GND278	E21
AM37	GND187	GND279	E25
AM38	GND188	GND280	E29
AM5	GND189	GND281	E33
AM6	GND190	GND282	F12
AM7	GND191	GND283	F16
AM9	GND192	GND284	F32
AP26	GND193	GND285	F8
AN28	GND194	GND286	G10
AN30	GND195	GND287	G12
AN39	GND196	GND288	G14
AN4	GND197	GND289	G16
Y7	GND198	GND290	BC12
AP10	GND199	GND291	G22
AU26	GND200	GND292	G24
AP14	GND201	GND293	AW20
AU14	GND202	GND294	G34
AP28	GND203	GND295	G4
AP32	GND204	GND296	G43
AP34	GND205	GND297	G6
AP36	GND206	GND298	G8
AP37	GND207	GND299	H11
AP4	GND208	GND300	H15
AP40	GND209	GND301	AW35
AP7	GND210	GND302	H23
AW23	GND211	GND303	AN8
AR28	GND212	GND304	G40
AR32	GND213	GND305	J12
AR40	GND214	GND306	J8
AT10	GND215	GND307	K10
AR12	GND216	GND308	K12
AT13	GND217	GND309	K18
AT29	GND218	GND310	K26
AT33	GND219	GND311	K37
AT6	GND220	GND312	K4
AT7	GND221	GND313	K40
AT9	GND222	GND314	K8
AY21	GND223	GND315	AU1
AY22	GND224	GND316	L40
L12	GND225	GND317	L43
AU12	GND226	GND318	L5
AU28	GND227	GND319	M10
AP33	GND228	GND320	M34
AU32	GND229	GND321	M35
AR30	GND230	GND322	M37
AU36	GND231	GND323	Y28
AU38	GND232	GND324	Y33
AU4	GND233	GND325	Y34
G28	GND234	GND326	Y35
F20	GND235	GND327	Y37
AV28	GND236	GND328	Y38
AV32	GND237	GND329	AB17
AV36	GND238	GND330	AB16
AV4	GND239	GND331	AN26
AV7	GND240	GND332	AD7
AW11	GND241	GND333	M11
G20	GND242	GND334	AA4
AR43	GND243	GND335	AB19
AW43	GND244	GND336	AY13
AY10	GND245	GND337	P11
AV12	GND246	GND338	Y6
AY30	GND247	GND339	T11
AY33	GND248	GND340	V11
AY34	GND249	GND341	Y11
AY37	GND250	GND342	AH16
AY38	GND251	GND343	T22
AY41	GND252		

OMIT

U1400
MCP79-TOPO-B
BGA
(10 OF 11)

POWER

25D8 6D4 =PPVCORE_S0_MCP
23065 mA (A01, 1.2V)
16996 mA (A01, 1.0V)

AA25	+VDD_CORE1	+VTT_CPU1	R32
AC23	+VDD_CORE2	+VTT_CPU2	AC32
U25	+VDD_CORE3	+VTT_CPU3	E40
AH12	+VDD_CORE4	+VTT_CPU4	J36
AG10	+VDD_CORE5	+VTT_CPU5	N32
AG5	+VDD_CORE6	+VTT_CPU6	T32
Y21	+VDD_CORE7	+VTT_CPU7	U32
Y23	+VDD_CORE8	+VTT_CPU8	V32
AA16	+VDD_CORE9	+VTT_CPU9	W32
AA26	+VDD_CORE10	+VTT_CPU10	P31
AA27	+VDD_CORE11	+VTT_CPU11	AF32
AA28	+VDD_CORE12	+VTT_CPU12	AE32
AC16	+VDD_CORE13	+VTT_CPU13	AH32
AC17	+VDD_CORE14	+VTT_CPU14	AJ32
AC18	+VDD_CORE15	+VTT_CPU15	AK31
AC19	+VDD_CORE16	+VTT_CPU16	AK32
AC20	+VDD_CORE17	+VTT_CPU17	AD32
AC21	+VDD_CORE18	+VTT_CPU18	AL31
AA17	+VDD_CORE19	+VTT_CPU19	AB32
AC24	+VDD_CORE20	+VTT_CPU20	B41
AC25	+VDD_CORE21	+VTT_CPU21	B42
AC26	+VDD_CORE22	+VTT_CPU22	C40
AC27	+VDD_CORE23	+VTT_CPU23	C41
AC28	+VDD_CORE24	+VTT_CPU24	C42
AD21	+VDD_CORE25	+VTT_CPU25	D39
AD23	+VDD_CORE26	+VTT_CPU26	D40
W27	+VDD_CORE27	+VTT_CPU27	D41
V25	+VDD_CORE28	+VTT_CPU28	E38
AA18	+VDD_CORE29	+VTT_CPU29	E39
AE19	+VDD_CORE30	+VTT_CPU30	F37
AE21	+VDD_CORE31	+VTT_CPU31	F38
AE23	+VDD_CORE32	+VTT_CPU32	F39
AE25	+VDD_CORE33	+VTT_CPU33	G36
AE26	+VDD_CORE34	+VTT_CPU34	G37
AE27	+VDD_CORE35	+VTT_CPU35	G38
AE28	+VDD_CORE36	+VTT_CPU36	H35
AF10	+VDD_CORE37	+VTT_CPU37	H37
AF11	+VDD_CORE38	+VTT_CPU38	J34
AA19	+VDD_CORE39	+VTT_CPU39	J35
AF2	+VDD_CORE40	+VTT_CPU40	K33
AF21	+VDD_CORE41	+VTT_CPU41	K34
AF23	+VDD_CORE42	+VTT_CPU42	K35
AF25	+VDD_CORE43	+VTT_CPU43	L32
AF3	+VDD_CORE44	+VTT_CPU44	L33
AF4	+VDD_CORE45	+VTT_CPU45	L34
AF7	+VDD_CORE46	+VTT_CPU46	M31
AH23	+VDD_CORE47	+VTT_CPU47	M32
AF9	+VDD_CORE48	+VTT_CPU48	M33
AA20	+VDD_CORE49	+VTT_CPU49	N31
AG11	+VDD_CORE50	+VTT_CPU50	P32
AG12	+VDD_CORE51	+VTT_CPU51	Y32
AG21	+VDD_CORE52	+VTT_CPU52	AA32
AG23	+VDD_CORE53		
AG25	+VDD_CORE54	+VTT_CPUCLK	AG32
AG3	+VDD_CORE55		
AG4	+VDD_CORE56		
AA21	+VDD_CORE57		
AG6	+VDD_CORE58		
AG7	+VDD_CORE59	+3.3V_1	AD10
AG8	+VDD_CORE60	+3.3V_2	AE8
AG9	+VDD_CORE61	+3.3V_3	AB10
AH1	+VDD_CORE62	+3.3V_4	AD9
AH10	+VDD_CORE63	+3.3V_5	Y10
AH11	+VDD_CORE64	+3.3V_6	AB11
W26	+VDD_CORE65	+3.3V_7	AA8
AH2	+VDD_CORE66	+3.3V_8	Y9
AA23	+VDD_CORE67		
W28	+VDD_CORE68		
AH25	+VDD_CORE69		
AH21	+VDD_CORE70	+3.3V_DUAL1	G10
AH3	+VDD_CORE71	+3.3V_DUAL2	H19
AH4	+VDD_CORE72	+3.3V_DUAL3	J20
AH5	+VDD_CORE73	+3.3V_DUAL4	K20
AH6	+VDD_CORE74		
AH7	+VDD_CORE75	+3.3V_DUAL_USB1	G26
AH9	+VDD_CORE76	+3.3V_DUAL_USB2	H27
AA24	+VDD_CORE77	+3.3V_DUAL_USB3	J28
W21	+VDD_CORE78	+3.3V_DUAL_USB4	K28
W23	+VDD_CORE79		
W25	+VDD_CORE80		
AF12	+VDD_CORE81		
A20	+VBAT	+VDD_AUXC1	T21
		+VDD_AUXC2	U21
		+VDD_AUXC3	V21

=PP1V05_S0_MCP_FSB
1139 mA
6D4 14A2 14B7 23C3 25C8
1182 mA (A01)

=PP3V3_S0_MCP
6B4 21C2 25B8
450 mA (A01)

=PP3V3_S5_MCP
6D1 25B8
16 mA
266 mA (A01)

250 mA

43 mA

=PP1V05_S5_MCP_VDD_AUXC
6D1 25D8
105 mA (A01)

28D5 21C8 PP3V3_G3_RTC
10 uA (G3)
80 uA (S0)

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MCP Power & Ground

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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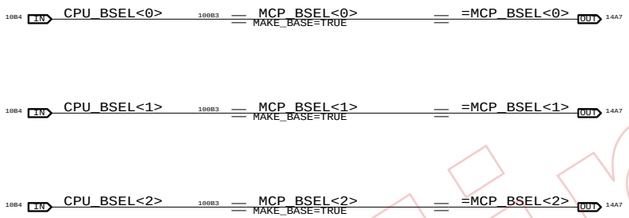
D	051-7840	10

SCALE	SHT	OF
NONE	22	109

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

CPU FSB Frequency Straps

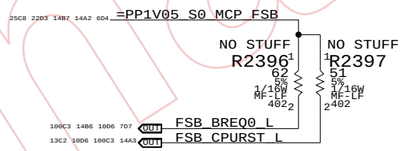


BSEL<2..0>	FSB MHz
000	266
001	133
010	200
011	(166)
100	333
101	100
110	(400)
111	(RSVD)

NOTE: () values not supported by MCP79.

Extra FSB Pull-ups

Exist in MRB but not Intel designs. Here for CYA.
If found to be necessary, will move to page14.csa



Merom/Penryn do not officially support PECI, but it's not clear whether PECI interface is present or not. T12 used pin F6.

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Debug: CPU

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7840	10

SCALE	SHT	OF
NONE	23	109

Preliminary
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MCP Core Power

=PPVCORE_S0_MCP

23065 mA (A01, 1.2V)
16996 mA (A01, 1.0V)

(No IG vs. EG data)

NV: 1x 10uF 0805, 2x 4.7uF 0402, 3x 1uF 0402, 9x 0.1uF 0402 (23.3 uF)
APPLE: 4X 4.7UF 0402, 4X 1UF 0402, 6X 0.1UF 0402 (23.4 UF)

C2500 4.7UF 20% 4V X5R 402
C2501 4.7UF 20% 4V X5R 402
C2502 4.7UF 20% 4V X5R 402
C2503 4.7UF 20% 4V X5R 402
C2504 1UF 10% 10V X5R 402-1
C2505 1UF 10% 10V X5R 402-1
C2506 1UF 10% 10V X5R 402-1
C2507 1UF 10% 10V X5R 402-1
C2508 0.1UF 20% 10V CERM 402
C2509 0.1UF 20% 10V CERM 402
C2510 0.1UF 20% 10V CERM 402
C2511 0.1UF 20% 10V CERM 402
C2512 0.1UF 20% 10V CERM 402
C2513 0.1UF 20% 10V CERM 402

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S0004	2	RES,0,5%,0402	C2574,C2518	IG

MCP PCIE (DVDD) Power
DIFFERENT THAN ON T18

=PP1V05_S0_MCP_PEX_DVDD

57 mA (A01)

PEX_DVDD RAIL SPLIT BASED ON TG VS. EG, 8 OUT OF 10 RAILS FOR DVDD SO 80% OF CAPACITANCE ON DVDD0

NV: 1X 4.7UF 0402, 2X 1UF 0402, 2X 0.1UF 0402 (6.9UF)
K50: 2X 2.2UF 0402, 2X 1UF 0402, (6.4 UF)

C2516 1UF 10% 10V X5R 402-1
C2515 2.2UF 20% 6.3V CERM 402-LF
C2517 1UF 10% 10V X5R 402-1
C2518 2.2UF 20% 6.3V CERM 402-LF

MCP SATA (DVDD) Power

=PP1V05_S0_MCP_SATA_DVDD

43 mA (A01)

C2520 4.7UF 20% 4V X5R 402
C2521 0.1UF 20% 10V CERM 402

MCP 1.05V AUX Power

=PP1V05_S5_MCP_VDD_AUXC

105 mA (A01)

C2525 0.1UF 20% 10V CERM 402
C2526 0.1UF 20% 10V CERM 402

MCP 1.05V RMGT Power

=PP1V05_ENET_MCP_RMGT

131 mA (A01)

C2528 4.7UF 20% 4V X5R 402
C2529 0.1UF 20% 10V CERM 402

MCP FSB (VTT) Power

=PP1V05_S0_MCP_FSB

1182 mA (A01)

NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 0.1uF 0402 (14.9 uF)
Apple: 7x 2.2uF 0402 (15.4 uF)

C2530 2.2UF 20% 6.3V CERM 402-LF
C2531 2.2UF 20% 6.3V CERM 402-LF
C2532 2.2UF 20% 6.3V CERM 402-LF
C2533 2.2UF 20% 6.3V CERM 402-LF
C2534 2.2UF 20% 6.3V CERM 402-LF
C2535 2.2UF 20% 6.3V CERM 402-LF
C2536 2.2UF 20% 6.3V CERM 402-LF

MCP Memory Power

=PP1V8R1V5_S0_MCP_MEM

4771 mA (A01, DDR3)

C2540 4.7UF 20% 4V X5R 402
C2541 0.1UF 20% 10V CERM 402
C2542 0.1UF 20% 10V CERM 402
C2543 0.1UF 20% 10V CERM 402
C2544 0.1UF 20% 10V CERM 402
C2545 0.1UF 20% 10V CERM 402
C2546 0.1UF 20% 10V CERM 402
C2547 0.1UF 20% 10V CERM 402
C2548 0.1UF 20% 10V CERM 402
C2549 0.1UF 20% 10V CERM 402

MCP 3.3V Power

=PP3V3_S0_MCP

450 mA (A01)

NV: 1x 4.7uF 0603, 4x 0.1uF 0402 (5.1 uF)
Apple: 4x 2.2uF 0402 (8.8 uF)

C2550 2.2UF 20% 6.3V CERM 402-LF
C2551 2.2UF 20% 6.3V CERM 402-LF
C2552 2.2UF 20% 6.3V CERM 402-LF
C2553 2.2UF 20% 6.3V CERM 402-LF

=PP3V3_S0_MCP_PLL_UF

19 mA (A01)

L2555 30-OHM-1.7A 0402

PP3V3_S0_MCP_PLL_USB
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
19 mA (A01)

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

C2555 2.2UF 20% 6.3V CERM 402-LF

MCP 3.3V AUX/USB Power

=PP3V3_S5_MCP

266 mA (A01)

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

C2560 2.2UF 20% 6.3V CERM 402-LF

MCP 3.3V Ethernet Power

=PP3V3_ENET_MCP_RMGT

83 mA (A01)

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

C2564 2.2UF 20% 6.3V CERM 402-LF

MCP 3.3V/1.5V HDA Power

=PP3V3R1V5_S0_MCP_HDA

7 mA (A01)

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

C2562 2.2UF 20% 6.3V CERM 402-LF

MCP79 Ethernet VRef

=PP3V3_ENET_MCP_RMGT

R2591 1.47K 1% 1/16W MF-LF 402
R2590 1.47K 1% 1/16W MF-LF 402

MCP_MII_VREF OUT

C2591 0.1UF 20% 10V CERM 402

=PP1V05_ENET_MCP_PLL_MAC

5 mA (A01)

L2595 30-OHM-1.7A 0402

PP1V05_ENET_MCP_PLL_MAC
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
5 mA (A01)

C2595 4.7UF 20% 4V X5R 402
C2596 0.1UF 20% 10V CERM 402

=PP1V05_S0_MCP_AVDD_UF

333 mA (A01)

NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 1uF 0402, 2x 0.1uF 0402 (16.9 uF)
Apple: 5x 2.2uF 0402 (11 uF)

L2570 30-OHM-5A 0603

PP1V05_S0_MCP_PEX_AVDD
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
206 mA (A01)

C2570 2.2UF 20% 6.3V CERM 402-LF
C2571 2.2UF 20% 6.3V CERM 402-LF
C2572 2.2UF 20% 6.3V CERM 402-LF
C2573 2.2UF 20% 6.3V CERM 402-LF
C2574 2.2UF 20% 6.3V CERM 402-LF

=PP1V05_S0_MCP_PEX_AVDD0

PEX_AVDD RAIL SPLIT BASED ON TG VS. EG, 10 OUT OF 15 RAILS FOR AVDD0 SO 80% OF CAPACITANCE ON AVDD0

NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 0.1uF 0402 (14.9 uF)
Apple: 2x 2.2uF 0402 (4.4 uF)

L2575 30-OHM-5A 0603

PP1V05_S0_MCP_SATA_AVDD
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
127 mA (A01)

C2575 2.2UF 20% 6.3V CERM 402-LF
C2576 2.2UF 20% 6.3V CERM 402-LF

=PP1V05_S0_MCP_PLL_UF

562 mA (A01)

L2580 30-OHM-1.7A 0402

PP1V05_S0_MCP_PLL_FSB
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
270 mA (A01)

C2580 4.7UF 20% 4V X5R 402
C2581 2.2UF 20% 4V X5R 402

L2582 30-OHM-1.7A 0402

PP1V05_S0_MCP_PLL_PEX
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
84 mA (A01)

C2582 4.7UF 20% 4V X5R 402
C2583 2.2UF 20% 4V X5R 402

L2584 30-OHM-1.7A 0402

PP1V05_S0_MCP_PLL_SATA
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
84 mA (A01)

C2584 4.7UF 20% 4V X5R 402
C2585 2.2UF 20% 4V X5R 402

L2586 30-OHM-1.7A 0402

PP1V05_S0_MCP_PLL_CORE
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
87 mA (A01)

C2586 4.7UF 20% 4V X5R 402
C2597 4.7UF 20% 4V X5R 402
C2587 2.2UF 20% 4V X5R 402

L2588 30-OHM-1.7A 0402

PP1V05_S0_MCP_PLL_NV
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
37 mA (A01)

C2588 4.7UF 20% 4V X5R 402
C2589 2.2UF 20% 4V X5R 402
C2590 2.2UF 20% 4V X5R 402

MCP Standard Decoupling

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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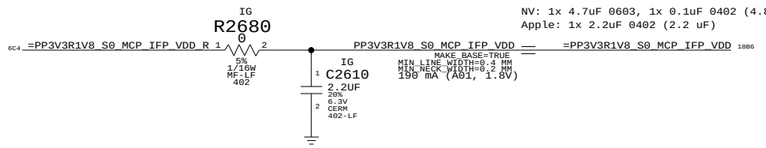
SIZE	DRAWING NUMBER	REV.
D	051-7840	10
SCALE: NONE	SHT 25 OF 109	

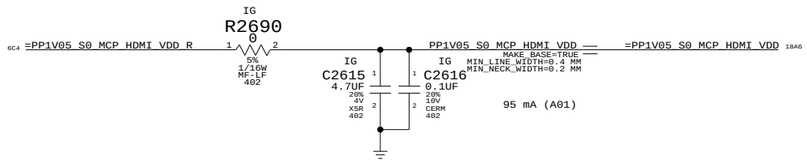
Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

WF: Checklist says 0-ohm resistor placeholder for ferrite bead.

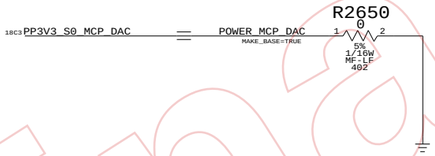
NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

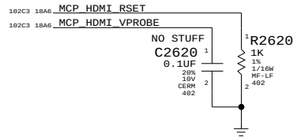


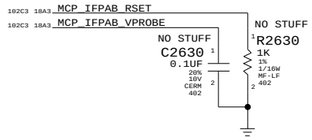
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S0004	1	RES,0,5%,402	C2610		MXM



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S0004	1	RES,0,5%,402	C2616		MXM

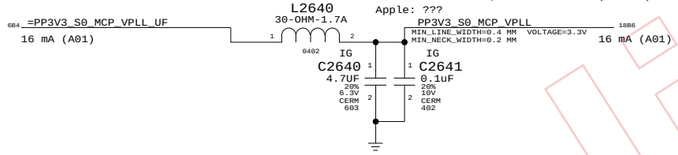






WF: Checklist says 0-ohm resistor placeholder for ferrite bead.

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: ???



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S0004	1	RES,0,5%,402	C2641		MXM

Preliminary

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP Graphics Support

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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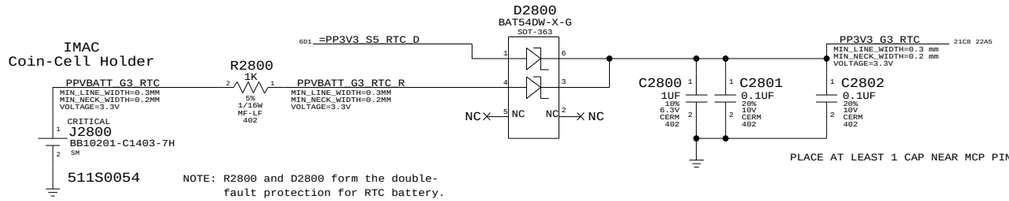
SIZE	DRAWING NUMBER	REV.
D	051-7840	10

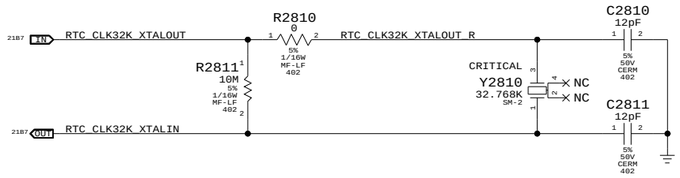
SCALE	SHT	OF
NONE	26	109

RTC Power Sources

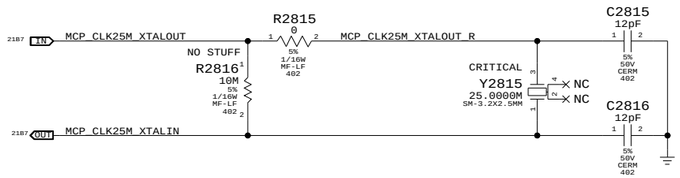


NOTE: R2800 and D2800 form the double-fault protection for RTC battery.

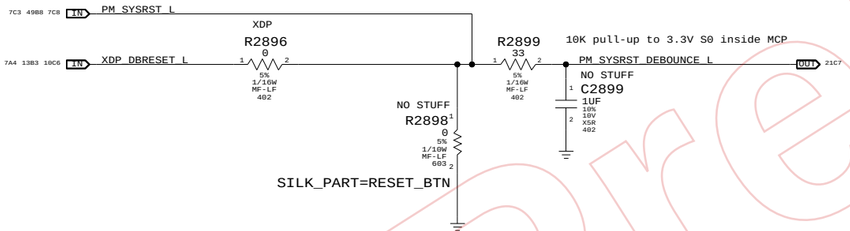
RTC Crystal



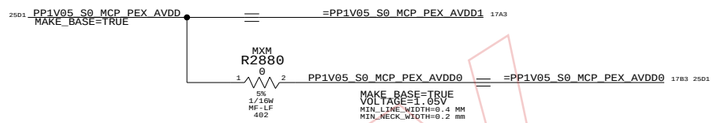
MCP 25MHz Crystal



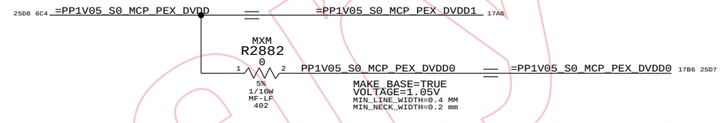
Reset Button



PEG POWER ALIAS/OPTION TO GND UNUSED POWER PIN

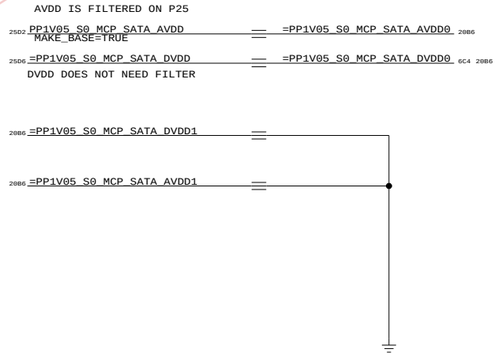


UNPOWER PEG INTERFACE WHEN IG IS USED



UNPOWER PEG INTERFACE WHEN IG IS USED

SATA ALIAS/GROUNDING UNUSED DVDD1 AND AVDD1



Preliminary

SB Misc

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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SIZE	DRAWING NUMBER	REV.
D	051-7840	10

SCALE	SHT	OF
NONE	28	109

Page Notes

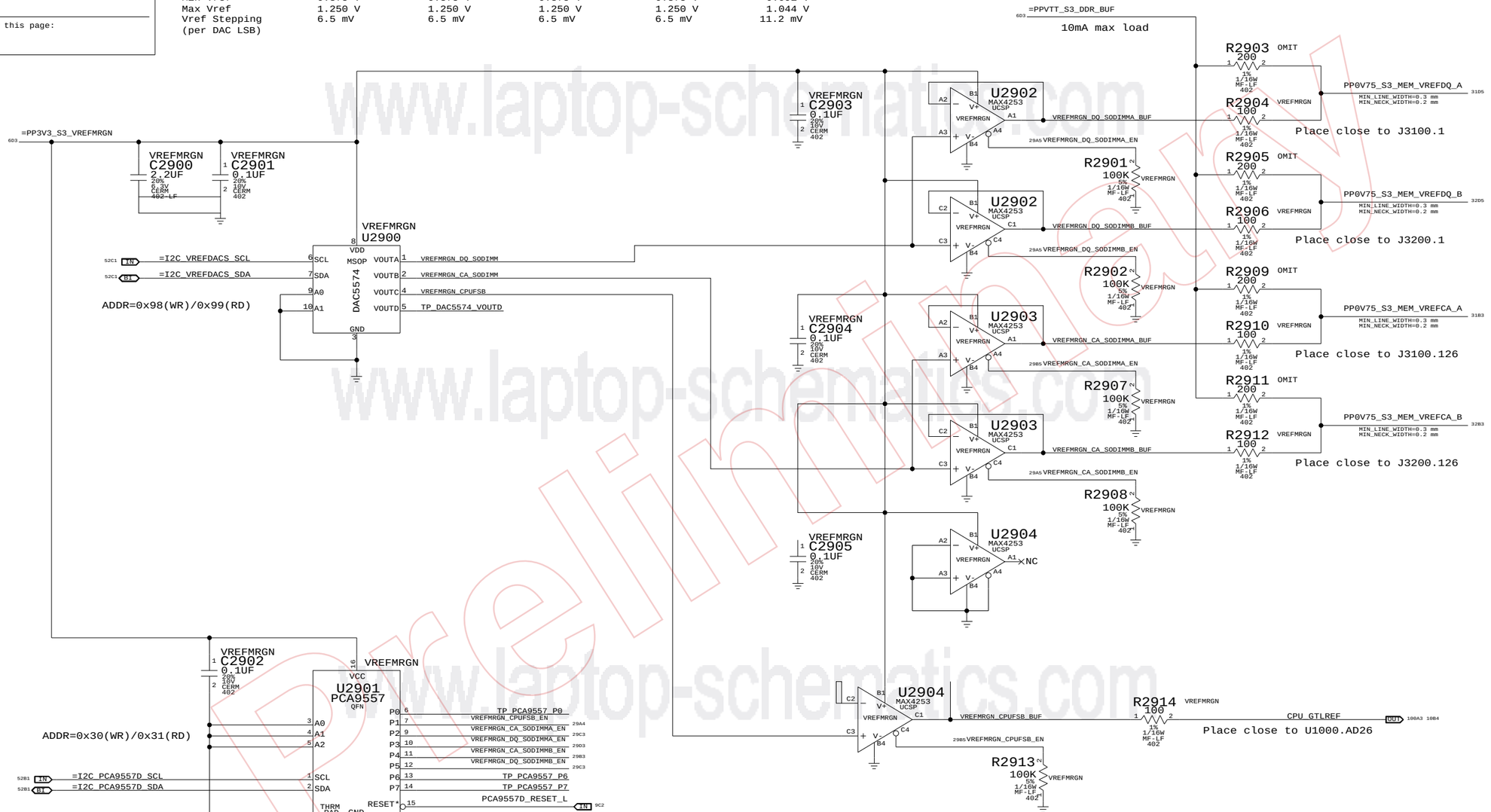
Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PP3V3_S5_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN
NO_VREFMRGN

DAC channel	MEM A VREF DQ A	MEM A VREF CA B	MEM B VREF DQ A	MEM B VREF CA B	CPU FSB VREF C
Min DAC code	0x00	0x00	0x00	0x00	0x00
Max DAC code	0x87	0x87	0x87	0x87	0x55
Max sink I	-3.75 mA	-3.75 mA	-3.75 mA	-3.75 mA	-0.91 mA
Max source I	5 mA	5 mA	5 mA	5 mA	0.52 mA
Nominal Vref	0.75 V	0.75 V	0.75 V	0.75 V	0.70 V
Min Vref	0.375 V	0.375 V	0.375 V	0.375 V	0.091 V
Max Vref	1.250 V	1.250 V	1.250 V	1.250 V	1.044 V
Vref Stepping (per DAC LSB)	6.5 mV	6.5 mV	6.5 mV	6.5 mV	11.2 mV

SO-DIMM A and SO-DIMM B Vref settings should be margined separately
(i.e. not simultaneously) due to current limitation of TPS51116 regulator.



Required zero ohm resistors when no VREF margining circuit stuffed

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S0149	1	RES,402,1/16W,200 OHM,1%	R2903		VREFMRGN
116S0004	1	RES,402,1/16W,0 OHM,5%	R2903		PRODUCTION
114S0149	1	RES,402,1/16W,200 OHM,1%	R2905		VREFMRGN
116S0004	1	RES,402,1/16W,0 OHM,5%	R2905		PRODUCTION
114S0149	1	RES,402,1/16W,200 OHM,1%	R2909		VREFMRGN
116S0004	1	RES,402,1/16W,0 OHM,5%	R2909		PRODUCTION
114S0149	1	RES,402,1/16W,200 OHM,1%	R2911		VREFMRGN
116S0004	1	RES,402,1/16W,0 OHM,5%	R2911		PRODUCTION

FSB/DDR3 Vref Margining

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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D	051-7840	10

SCALE: NONE SHT: 29 OF: 109

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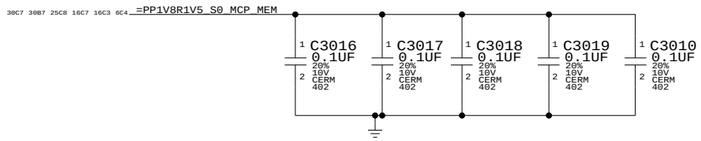
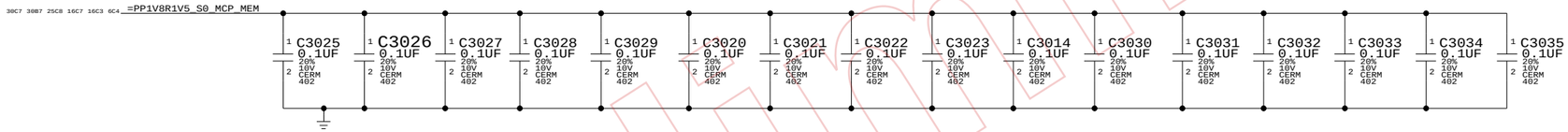
Preliminary

CAPS TO COUPLE MCP 1V5_S0_MEM AND DIMMS 1V5_S3

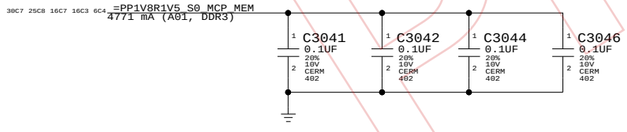
CAPS TO COUPLE MCP 1V5_S0_MEM ON DIMM A (FURTHER FROM MCP)



CAPS TO COUPLE MCP 1V5_S0_MEM ON DIMM B (CLOSER TO MCP)



EXTRA DECOUPLING CAPS FOR MCP MEM RAIL



Preliminary

MEMORY COUPLING CAPS

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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SIZE	DRAWING NUMBER	REV.
D	051-7840	10

SCALE	SHT	OF
NONE	30	109

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

DDR3 DECOUPLING AND GROUND RETURN CAPS (CONNECTOR SIDE)

31A5 108D3 6D3 =PP1V5_S3_MEM_A

C3100 10UF 20% 6.3V X5R 603
C3101 10UF 20% 6.3V X5R 603
C3110 1UF 10% 6.3V CERM 402
C3111 1UF 10% 6.3V CERM 402
C3112 1UF 10% 6.3V CERM 402
C3113 1UF 10% 6.3V CERM 402
C3114 1UF 10% 6.3V CERM 402
C3115 1UF 10% 6.3V CERM 402
C3116 1UF 10% 6.3V CERM 402
C3117 1UF 10% 6.3V CERM 402
C3118 1UF 10% 6.3V CERM 402
C3119 1UF 10% 6.3V CERM 402
C3120 1UF 10% 6.3V CERM 402
C3121 1UF 10% 6.3V CERM 402
C3122 1UF 10% 6.3V CERM 402
C3123 1UF 10% 6.3V CERM 402

29D1 PP0V75_S3_MEM_VREFDQ_A

C3130 2.2UF 20% 6.3V CERM 402-LF
C3131 0.1UF 20% 10V CERM 402

CRITICAL

J3100 DDR3-SODIMM (SYMBOL 2 OF 2) F-RT-SM

101D3 15A5	IN	MEM_A_CKE<0>	73	CKE0	CKE1	74	MEM_A_CKE<1>	IN	15A5 101D3
			75	VDD	VDD	76			
NC			77	NC	A15	78	MEM_A_A<15>	IN	8C4
101D3 15C5	IN	MEM_A_BA<2>	79	BA2	A14	80	MEM_A_A<14>	IN	15C5 101D3
			81	VDD	VDD	82			
101D3 15C5	IN	MEM_A_A<12>	83	A12/BC*	A11	84	MEM_A_A<11>	IN	15C5 101D3
101D3 15C5	IN	MEM_A_A<9>	85	A9	A7	86	MEM_A_A<7>	IN	15C5 101D3
			87	VDD	VDD	88			
101D3 15C5	IN	MEM_A_A<8>	89	A8	A6	90	MEM_A_A<6>	IN	15B5 101D3
101D3 15B5	IN	MEM_A_A<5>	91	A5	A4	92	MEM_A_A<4>	IN	15B5 101D3
			93	VDD	VDD	94			
101D3 15B5	IN	MEM_A_A<3>	95	A3	A2	96	MEM_A_A<2>	IN	15B5 101D3
101D3 15B5	IN	MEM_A_A<1>	97	A1	A0	98	MEM_A_A<0>	IN	15B5 101D3
			99	VDD	VDD	100			
101D3 15B5	IN	MEM_A_CLK_P<0>	101	CK0	CK1	102	MEM_A_CLK_P<1>	IN	15B5 101D3
101D3 15B5	IN	MEM_A_CLK_N<0>	103	CK0*	CK1*	104	MEM_A_CLK_N<1>	IN	15B5 101D3
			105	VDD	VDD	106			
101D3 15C5	IN	MEM_A_A<10>	107	A10/AP	BA1	108	MEM_A_BA<1>	IN	15C5 101D3
101D3 15C5	IN	MEM_A_BA<0>	109	BA0	RAS*	110	MEM_A_RAS_L	IN	15C5 101D3
			111	VDD	VDD	112			
101D3 15C5	IN	MEM_A_WE_L	113	WE*	S0*	114	MEM_A_CS_L<0>	IN	15B5 101D3
101D3 15C5	IN	MEM_A_CAS_L	115	CAS*	ODT0	116	MEM_A_ODT<0>	IN	15B5 101D3
			117	VDD	VDD	118			
101D3 15C5	IN	MEM_A_A<13>	119	A13	ODT1	120	MEM_A_ODT<1>	IN	15B5 101D3
101D3 15B5	IN	MEM_A_CS_L<1>	121	S1*	NC	122			
			123	VDD	VDD	124			
NC			125	TEST	VREFCA	126			
			127	VSS	VSS	128			
101C3 15C7	BI	MEM_A_DQ<32>	129	DQ32	DQ36	130	MEM_A_DQ<37>	BI	15C7 101C3
101C3 15C7	BI	MEM_A_DQ<33>	131	DQ33	DQ37	132	MEM_A_DQ<36>	BI	15C7 101C3
			133	VSS	VSS	134			
101C3 15D5	BI	MEM_A_DQS_N<4>	135	DQS4*	DM4	136	MEM_A_DM<4>	IN	15B7 101C3
101C3 15D5 7B7	BI	MEM_A_DQS_P<4>	137	DQS4	VSS	138			
			139	VSS	DQ38	140	MEM_A_DQ<35>	BI	15C7 101C3
101C3 15C7	BI	MEM_A_DQ<34>	141	DQ34	DQ39	142	MEM_A_DQ<39>	BI	15C7 101C3
101C3 15C7	BI	MEM_A_DQ<38>	143	DQ35	VSS	144			
			145	VSS	DQ44	146	MEM_A_DQ<40>	BI	15C7 101C3
101C3 15C7	BI	MEM_A_DQ<44>	147	DQ40	DQ45	148	MEM_A_DQ<41>	BI	15C7 101C3
101C3 15C7	BI	MEM_A_DQ<45>	149	DQ41	VSS	150			
			151	VSS	DQS5*	152	MEM_A_DQS_N<5>	BI	15D5 101C3
101C3 15B7	IN	MEM_A_DM<5>	153	DM5	DQS5	154	MEM_A_DQS_P<5>	BI	7B7 15D5 101C3
			155	VSS	VSS	156			
101C3 15D7 7C7	BI	MEM_A_DQ<47>	157	DQ42	DQ46	158	MEM_A_DQ<43>	BI	15C7 101C3
101C3 15D7	BI	MEM_A_DQ<46>	159	DQ43	DQ47	160	MEM_A_DQ<42>	BI	15C7 101C3
			161	VSS	VSS	162			
101C3 15D7	BI	MEM_A_DQ<49>	163	DQ48	DQ52	164	MEM_A_DQ<53>	BI	15D7 101C3
101C3 15D7	BI	MEM_A_DQ<52>	165	DQ49	DQ53	166	MEM_A_DQ<48>	BI	15D7 101C3
			167	VSS	VSS	168			
101B3 15D5 7B7	BI	MEM_A_DQS_N<6>	169	DQS6*	DM6	170	MEM_A_DM<6>	IN	15B7 101C3
101B3 15D5	BI	MEM_A_DQS_P<6>	171	DQS6	VSS	172			
			173	VSS	DQ54	174	MEM_A_DQ<50>	BI	15D7 101C3
101C3 15D7	BI	MEM_A_DQ<54>	175	DQ50	DQ55	176	MEM_A_DQ<55>	BI	15D7 101C3
101C3 15D7	BI	MEM_A_DQ<51>	177	DQ51	VSS	178			
			179	VSS	DQ60	180	MEM_A_DQ<57>	BI	15D7 101C3
101C3 15D7	BI	MEM_A_DQ<61>	181	DQ56	DQ61	182	MEM_A_DQ<56>	BI	15D7 101C3
101C3 15D7	BI	MEM_A_DQ<60>	183	DQ57	VSS	184			
			185	VSS	DQS7*	186	MEM_A_DQS_N<7>	BI	15D5 101B3
101C3 15B7	IN	MEM_A_DM<7>	187	DM7	DQS7	188	MEM_A_DQS_P<7>	BI	15D5 101B3
			189	VSS	VSS	190			
101C3 15D7	BI	MEM_A_DQ<58>	191	DQ58	DQ62	192	MEM_A_DQ<62>	BI	15D7 101C3
101C3 15D7 7C7	BI	MEM_A_DQ<59>	193	DQ59	DQ63	194	MEM_A_DQ<63>	BI	15D7 101C3
			195	VSS	VSS	196			
		MEM_A_SA<0>	197	SA0	EVENT*	198	MEM_EVENT_L	OUT	32A5 49B8 21A4 21B3 55C1
6B4 =PPSPD_S0_MEM_A			199	VDDSPD	SDA	200	=I2C_SODIMMA_SDA	BI	52D6
		MEM_A_SA<1>	201	SA1	SCL	202	=I2C_SODIMMA_SCL	IN	52D6
			203	VTT	VTT	204			=PP0V75_S0_MEM_VTT_A 6D4
			205	MTG PIN	MTG PIN	207			
			206	MTG PIN	MTG PIN	208	=PP1V5_S3_MEM_A 6D3 108D3 31D7		
			209	MTG PIN					

516S0657

SPD ADDR=0xA0(WR)/0xA1(RD)

C3140 2.2UF 20% 6.3V CERM 402-LF
R3140 10K 5% 1/16W MF-LF 402
R3141 10K 5% 1/16W MF-LF 402

J3100 DDR3-SODIMM (SYMBOL 1 OF 2) F-RT-SM

		VREFDQ	1	VSS	VSS	2	
101D3 15B7	BI	MEM_A_DQ<0>	3	DQ0	DQ4	4	MEM_A_DQ<4>	BI	15B7 101D3
101D3 15B7	BI	MEM_A_DQ<1>	5	DQ1	DQ5	6	MEM_A_DQ<5>	BI	15B7 101D3
			7	VSS	VSS	8			
101C3 15A7	IN	MEM_A_DM<0>	9	DM0	DQS0*	10	MEM_A_DQS_N<0>	BI	15D5 101C3
			11	VSS	DQS0	12	MEM_A_DQS_P<0>	BI	15D5 101C3
101D3 15B7	BI	MEM_A_DQ<6>	13	DQ2	VSS	14			
101D3 15B7 7C7	BI	MEM_A_DQ<7>	15	DQ3	DQ6	16	MEM_A_DQ<3>	BI	15B7 101D3
			17	VSS	DQ7	18	MEM_A_DQ<2>	BI	15B7 101D3
101D3 15B7	BI	MEM_A_DQ<8>	19	DQ8	VSS	20			
101D3 15B7	BI	MEM_A_DQ<12>	21	DQ9	DQ12	22	MEM_A_DQ<9>	BI	15B7 101D3
			23	VSS	DQ13	24	MEM_A_DQ<13>	BI	15B7 101D3
101C3 15D5	BI	MEM_A_DQS_N<1>	25	DQS1*	VSS	26			
101C3 15D5 7C7	BI	MEM_A_DQS_P<1>	27	DQS1	DM1	28	MEM_A_DM<1>	IN	15A7 101C3
			29	VSS	RESET*	30	MEM_RESET_L	IN	33C3 32C2
101D3 15B7	BI	MEM_A_DQ<10>	31	DQ10	VSS	32			
101D3 15B7	BI	MEM_A_DQ<15>	33	DQ11	DQ14	34	MEM_A_DQ<11>	BI	15B7 101D3
			35	VSS	DQ15	36	MEM_A_DQ<14>	BI	7C7 15B7 101D3
101D3 15C7 7C7	BI	MEM_A_DQ<25>	37	DQ16	VSS	38			
101D3 15C7	BI	MEM_A_DQ<24>	39	DQ17	DQ20	40	MEM_A_DQ<29>	BI	15C7 101D3
			41	VSS	DQ21	42	MEM_A_DQ<28>	BI	15C7 101D3
101C3 15D5	BI	MEM_A_DQS_N<3>	43	DQS2*	VSS	44			
101C3 15D5 7C7	BI	MEM_A_DQS_P<3>	45	DQS2	DM2	46	MEM_A_DM<3>	IN	15B7 101C3
			47	VSS	VSS	48			
101D3 15C7	BI	MEM_A_DQ<26>	49	DQ18	DQ22	50	MEM_A_DQ<27>	BI	15C7 101D3
101D3 15C7	BI	MEM_A_DQ<30>	51	DQ19	DQ23	52	MEM_A_DQ<31>	BI	15C7 101D3
			53	VSS	VSS	54			
101D3 15C7	BI	MEM_A_DQ<20>	55	DQ24	DQ28	56	MEM_A_DQ<18>	BI	15B7 101D3
101D3 15C7	BI	MEM_A_DQ<21>	57	DQ25	DQ29	58	MEM_A_DQ<17>	BI	15B7 101D3
			59	VSS	VSS	60			
101D3 15B7	IN	MEM_A_DM<2>	61	DQS3*	DQS3	62	MEM_A_DQS_N<2>	BI	15D5 101C3
			63	DM3	DQS3	64	MEM_A_DQS_P<2>	BI	7C7 15D5 101C3
101D3 15C7	BI	MEM_A_DQ<23>	65	VSS	VSS	66			
101D3 15B7 7C7	BI	MEM_A_DQ<16>	67	DQ26	DQ30	68	MEM_A_DQ<19>	BI	15B7 101D3
			69	DQ27	DQ31	70	MEM_A_DQ<22>	BI	15C7 101D3
			71	VSS	VSS	72			

KEY

PP0V75_S3_MEM_VREFCA_A 29C1

C3135 2.2UF 20% 6.3V CERM 402-LF
C3136 0.1UF 20% 10V CERM 402

C3150 2.2UF 20% 6.3V CERM 402-LF
C3151 2.2UF 20% 6.3V CERM 402-LF

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DDR3 SO-DIMM Connector A

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7840	10
SCALE: NONE	SHT 31 OF 109	

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

DDR3 DECOUPLING AND GROUND RETURN CAPS (CONNECTOR SIDE)

32A5 108D3 6D3 =PP1V5_S3_MEM_B

C3200 10UF 20% 6.3V X5R 603
C3201 10UF 20% 6.3V X5R 603
C3210 1UF 10% 6.3V CERM 402
C3211 1UF 10% 6.3V CERM 402
C3212 1UF 10% 6.3V CERM 402
C3213 1UF 10% 6.3V CERM 402
C3214 1UF 10% 6.3V CERM 402
C3215 1UF 10% 6.3V CERM 402
C3216 1UF 10% 6.3V CERM 402
C3217 1UF 10% 6.3V CERM 402
C3218 1UF 10% 6.3V CERM 402
C3219 1UF 10% 6.3V CERM 402
C3220 1UF 10% 6.3V CERM 402
C3221 1UF 10% 6.3V CERM 402
C3222 1UF 10% 6.3V CERM 402
C3223 1UF 10% 6.3V CERM 402

29C1 PP0V75_S3_MEM_VREFDQ_B

C3230 2.2UF 20% 6.3V CERM 402-LF
C3231 0.1UF 20% 10V CERM 402

CRITICAL
KEY
J3200 DDR3-SODIMM (SYMBOL 2 OF 2) F-RT-SM

101B3 15A1 IN	MEM_B_CKE<0>	73	CKE0	CKE1	74	MEM_B_CKE<1>	IN 15A1 101B3
		75	VDD	VDD	76		
NC		77	NC	A15	78	MEM_B_A<15>	IN 8C4
101B3 15C1 IN	MEM_B_BA<2>	79	BA2	A14	80	MEM_B_A<14>	IN 15C1 101B3
		81	VDD	VDD	82		
101B3 15C1 IN	MEM_B_A<12>	83	A12/BC*	A11	84	MEM_B_A<11>	IN 15C1 101B3
101B3 15C1 IN	MEM_B_A<9>	85	A9	A7	86	MEM_B_A<7>	IN 15C1 101B3
		87	VDD	VDD	88		
101B3 15C1 IN	MEM_B_A<8>	89	A8	A6	90	MEM_B_A<6>	IN 15B1 101B3
101B3 15B1 IN	MEM_B_A<5>	91	A5	A4	92	MEM_B_A<4>	IN 15B1 101B3
		93	VDD	VDD	94		
101B3 15B1 IN	MEM_B_A<3>	95	A3	A2	96	MEM_B_A<2>	IN 15B1 101B3
101B3 15B1 IN	MEM_B_A<1>	97	A1	A0	98	MEM_B_A<0>	IN 15B1 101B3
		99	VDD	VDD	100		
101B3 15B1 IN	MEM_B_CLK_P<0>	101	CK0	CK1	102	MEM_B_CLK_P<1>	IN 15B1 101B3
101B3 15B1 IN	MEM_B_CLK_N<0>	103	CK0*	CK1*	104	MEM_B_CLK_N<1>	IN 15B1 101B3
		105	VDD	VDD	106		
101B3 15C1 IN	MEM_B_A<10>	107	A10/AP	BA1	108	MEM_B_BA<1>	IN 15C1 101B3
101B3 15C1 IN	MEM_B_BA<0>	109	BA0	RAS*	110	MEM_B_RAS_L	IN 15C1 101B3
		111	VDD	VDD	112		
101B3 15C1 IN	MEM_B_WE_L	113	WE*	S0*	114	MEM_B_CS_L<0>	IN 15B1 101B3
101B3 15C1 IN	MEM_B_CAS_L	115	CAS*	ODT0	116	MEM_B_ODT<0>	IN 15B1 101B3
		117	VDD	VDD	118		
101B3 15C1 IN	MEM_B_A<13>	119	A13	ODT1	120	MEM_B_ODT<1>	IN 15B1 101B3
101B3 15B1 IN	MEM_B_CS_L<1>	121	S1*	NC	122		
		123	VDD	VDD	124		
NC		125	TEST	VREFCA	126		
		127	VSS	VSS	128		
101B3 15C3 BI	MEM_B_DQ<32>	129	DQ32	DQ36	130	MEM_B_DQ<37>	BI 15C3 101B3
101B3 15C3 BI	MEM_B_DQ<33>	131	DQ33	DQ37	132	MEM_B_DQ<36>	BI 15C3 101B3
		133	VSS	VSS	134		
101D1 15D1 7B7 BI	MEM_B_DQS_N<4>	135	DQS4*	DM4	136	MEM_B_DM<4>	IN 15B3 101A3
101D1 15D1 BI	MEM_B_DQS_P<4>	137	DQS4	VSS	138		
		139	VSS	DQ38	140	MEM_B_DQ<35>	BI 15C3 101B3
101B3 15C3 BI	MEM_B_DQ<34>	141	DQ34	DQ39	142	MEM_B_DQ<39>	BI 15C3 101A3
101A3 15C3 7B7 BI	MEM_B_DQ<38>	143	DQ35	VSS	144		
		145	VSS	DQ44	146	MEM_B_DQ<40>	BI 15C3 101A3
101A3 15C3 BI	MEM_B_DQ<44>	147	DQ40	DQ45	148	MEM_B_DQ<41>	BI 15C3 101A3
101A3 15C3 BI	MEM_B_DQ<45>	149	DQ41	VSS	150		
		151	VSS	DQS5*	152	MEM_B_DQS_N<5>	BI 7B7 15D1 101D1
101A3 15B3 IN	MEM_B_DM<5>	153	DM5	DQS5	154	MEM_B_DQS_P<5>	BI 7B7 15D1 101D1
		155	VSS	VSS	156		
101A3 15D3 BI	MEM_B_DQ<47>	157	DQ42	DQ46	158	MEM_B_DQ<43>	BI 15C3 101A3
101A3 15D3 BI	MEM_B_DQ<46>	159	DQ43	DQ47	160	MEM_B_DQ<42>	BI 15C3 101A3
		161	VSS	VSS	162		
101A3 15D3 BI	MEM_B_DQ<49>	163	DQ48	DQ52	164	MEM_B_DQ<53>	BI 15D3 101A3
101A3 15D3 BI	MEM_B_DQ<52>	165	DQ49	DQ53	166	MEM_B_DQ<48>	BI 15D3 101A3
		167	VSS	VSS	168		
101D1 15D1 BI	MEM_B_DQS_N<6>	169	DQS6*	DM6	170	MEM_B_DM<6>	IN 15B3 101A3
101D1 15D1 7B7 BI	MEM_B_DQS_P<6>	171	DQS6	VSS	172		
		173	VSS	DQ54	174	MEM_B_DQ<50>	BI 15D3 101A3
101A3 15D3 BI	MEM_B_DQ<54>	175	DQ50	DQ55	176	MEM_B_DQ<55>	BI 15D3 101A3
101A3 15D3 BI	MEM_B_DQ<51>	177	DQ51	VSS	178		
		179	VSS	DQ60	180	MEM_B_DQ<57>	BI 15D3 101A3
101A3 15D3 BI	MEM_B_DQ<61>	181	DQ56	DQ61	182	MEM_B_DQ<56>	BI 15D3 101A3
101A3 15D3 BI	MEM_B_DQ<60>	183	DQ57	VSS	184		
		185	VSS	DQS7*	186	MEM_B_DQS_N<7>	BI 7B7 15D1 101D1
101A3 15B3 IN	MEM_B_DM<7>	187	DM7	DQS7	188	MEM_B_DQS_P<7>	BI 15D1 101D1
		189	VSS	VSS	190		
101A3 15D3 BI	MEM_B_DQ<58>	191	DQ58	DQ62	192	MEM_B_DQ<62>	BI 7B7 15D3 101A3
101A3 15D3 BI	MEM_B_DQ<59>	193	DQ59	DQ63	194	MEM_B_DQ<63>	BI 15D3 101A3
		195	VSS	VSS	196		
		197	SA0	EVENT*	198	MEM_EVENT_L	OUT 31A5 49B8 21A4 21B3 55C1
		199	VDDSPD	SDA	200	=I2C_SODIMMB_SDA	BI 52D6
	MEM_B_SA<0>	201	SA1	SCL	202	=I2C_SODIMMB_SCL	IN 52D6
	MEM_B_SA<1>	203	VTT	VTT	204	=PP0V75_S0_MEM_VTT_B	6D4
		205	MTG PIN	MTG PIN	207		
		206	MTG PIN	MTG PIN	208	=PP1V5_S3_MEM_B	6D3 108D3 32D7
		209	MTG PIN				

516S0657
K50/K51: SPD ADDR=0XA2(WR)/0XA3(RD)
K9: SPD ADDR=0XA4(WR)/0XA5(RD)

6B4 =PPSPD_S0_MEM_B

R3240 10K 5% 1/16W MF-LF 402
C3240 2.2UF 20% 6.3V CERM 402-LF
R3241 10K 5% 1/16W MF-LF 402

J3200 DDR3-SODIMM (SYMBOL 1 OF 2) F-RT-SM

		1	VREFDQ	VSS	2		
101B3 15B3 BI	MEM_B_DQ<0>	3	VSS	DQ4	4	MEM_B_DQ<4>	BI 15B3 101B3
101B3 15B3 BI	MEM_B_DQ<1>	5	DQ0	DQ5	6	MEM_B_DQ<5>	BI 15B3 101B3
		7	DQ1	VSS	8		
101A3 15A3 IN	MEM_B_DM<0>	9	VSS	DQS0*	10	MEM_B_DQS_N<0>	BI 15D1 101D1
		11	DM0	DQS0	12	MEM_B_DQS_P<0>	BI 15D1 101D1
		13	VSS	VSS	14		
101B3 15B3 7B7 BI	MEM_B_DQ<6>	15	DQ2	DQ6	16	MEM_B_DQ<3>	BI 15B3 101B3
101B3 15B3 BI	MEM_B_DQ<7>	17	DQ3	DQ7	18	MEM_B_DQ<2>	BI 15B3 101B3
		19	VSS	VSS	20		
101B3 15B3 7B7 BI	MEM_B_DQ<8>	21	DQ8	DQ12	22	MEM_B_DQ<9>	BI 15B3 101B3
101B3 15B3 BI	MEM_B_DQ<12>	23	DQ9	DQ13	24	MEM_B_DQ<13>	BI 15B3 101B3
		25	VSS	VSS	26		
101D1 15D1 BI	MEM_B_DQS_N<1>	27	DQS1*	DM1	28	MEM_B_DM<1>	IN 15A3 101A3
101D1 15D1 BI	MEM_B_DQS_P<1>	29	DQS1	RESET*	30	MEM_RESET_L	IN 33C3 31C2
		31	VSS	VSS	32		
101B3 15B3 BI	MEM_B_DQ<10>	33	DQ10	DQ14	34	MEM_B_DQ<11>	BI 15B3 101B3
101B3 15B3 BI	MEM_B_DQ<15>	35	DQ11	DQ15	36	MEM_B_DQ<14>	BI 15B3 101B3
		37	VSS	VSS	38		
101B3 15C3 7B7 BI	MEM_B_DQ<25>	39	DQ16	DQ20	40	MEM_B_DQ<29>	BI 15C3 101B3
101B3 15C3 BI	MEM_B_DQ<24>	41	DQ17	DQ21	42	MEM_B_DQ<28>	BI 15C3 101B3
		43	VSS	VSS	44		
101D1 15D1 7B7 BI	MEM_B_DQS_N<3>	45	DQS2*	DM2	46	MEM_B_DM<3>	IN 15B3 101A3
101D1 15D1 BI	MEM_B_DQS_P<3>	47	DQS2	VSS	48		
		49	VSS	DQ22	50	MEM_B_DQ<27>	BI 15C3 101B3
101B3 15C3 BI	MEM_B_DQ<26>	51	DQ18	DQ23	52	MEM_B_DQ<31>	BI 15C3 101B3
101B3 15C3 BI	MEM_B_DQ<30>	53	DQ19	VSS	54		
		55	VSS	DQ28	56	MEM_B_DQ<18>	BI 15B3 101B3
101B3 15C3 BI	MEM_B_DQ<20>	57	DQ24	DQ29	58	MEM_B_DQ<17>	BI 15B3 101B3
101B3 15C3 BI	MEM_B_DQ<21>	59	DQ25	VSS	60		
		61	VSS	DQS3*	62	MEM_B_DQS_N<2>	BI 15D1 101D1
101A3 15B3 IN	MEM_B_DM<2>	63	DM3	DQS3	64	MEM_B_DQS_P<2>	BI 7B7 15D1 101D1
		65	VSS	VSS	66		
101B3 15C3 7B7 BI	MEM_B_DQ<23>	67	DQ26	DQ30	68	MEM_B_DQ<19>	BI 15B3 101B3
101B3 15B3 BI	MEM_B_DQ<16>	69	DQ27	DQ31	70	MEM_B_DQ<22>	BI 15C3 101B3
		71	VSS	VSS	72		

KEY

PP0V75_S3_MEM_VREFCA_B 29C1

C3235 2.2UF 20% 6.3V CERM 402-LF
C3236 0.1UF 20% 10V CERM 402

C3250 2.2UF 20% 6.3V CERM 402-LF
C3251 2.2UF 20% 6.3V CERM 402-LF

DDR3 SO-DIMM CONNECTOR B

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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SIZE	DRAWING NUMBER	REV.
D	051-7840	10
SCALE	SHT	OF
NONE	32	109

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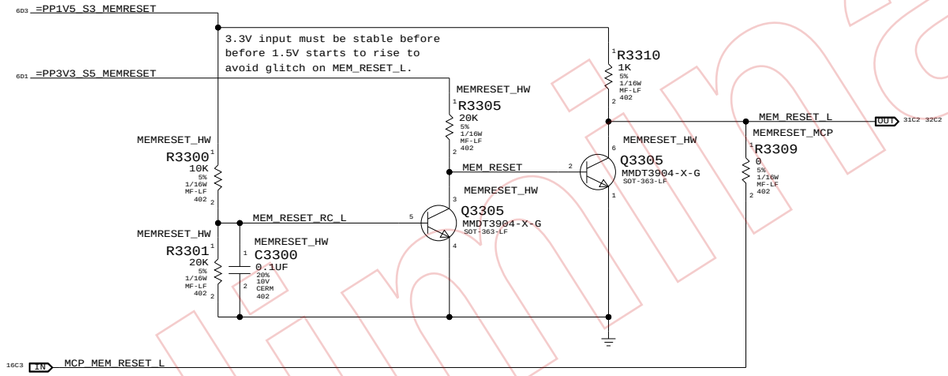
DDR3 RESET Support

MCP79 cannot control this signal directly since it must be high in sleep and MCP MEM rails are not powered in sleep.



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DDR3 Support

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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D	051-7840	10
SCALE: NONE	SHT 33 OF 109	

3.3V_S3_CURRENT	D0-D2_D3HOT	D3COLD
MAX CONT:	1100MA	100mA
MAX PEAK	2750MA	2750MA
1.5V_CURRENT		
MAX CONT:	N/U	N/U
MAX PEAK	N/U	N/U

NOTE: CURRENT DATA PER JAN 12,2008 PCIE MINI CEM ECN

NO STUFF
R3400
0
5%
1/16W
MF-LF
402

NO STUFF
R3401
0
5%
1/16W
MF-LF
402

CRITICAL
J3400
ASOB226-S80N-7F
F-RT-SM
516S0391

17B6 OUT	PCIE_WAKE_L	1	2
	RSVD_MINI_WLAN_ACTIVE	3	4
	RSVD_MINI_BT_ACTIVE	5	6
17C6 OUT	MINI_CLKREQ_L	7	8 NC
		9	10 NC
102C3 17C3 IN	PCIE_CLK100M_MINI_N	11	12 NC
102C3 17C3 IN	PCIE_CLK100M_MINI_P	13	14 NC
		15	16 NC
	RESERVED	NC 17	18
	RESERVED	NC 19	20 NC
		21	22 MINI_RESET_L IN 9C2
		23	24
		25	26
		27	28
		29	30 =SMBUS_MINI_SCL IN 52B3
		31	32 =SMBUS_MINI_SDA BI 52B3
		33	34
		35	36 USB_MINI_N BI 20D3 103C3
		37	38 USB_MINI_P BI 20D3 103C3
		39	40
		41	42 NC
		43	44 NC
	NC	45	46 NC
	NC	47	48
	NC	49	50
	NC	51	52
			53

17B6 102D3 7C8 OUT PCIE_MINI_D2R_N
17B6 102D3 7C8 OUT PCIE_MINI_D2R_P

PLACEMENT_NOTE=PLACE CLOSE TO U1400.
C3431
0.1uF
10%
16V
X5R
402

102D3 17B3 IN PCIE_MINI_R2D_C_N

PLACEMENT_NOTE=PLACE CLOSE TO U1400.
C3430
0.1uF
10%
16V
X5R
402

102D3 17B3 IN PCIE_MINI_R2D_C_P

102D3 PCIE_MINI_R2D_N
102D3 PCIE_MINI_R2D_P

=PP3V3_S3_MINI 6D3

C3410 0.1uF 20% 10V CERM 402
C3420 0.1uF 20% 10V CERM 402
C3421 10uF 20% 6.3V X5R 603

=PP1V5_S0_MINI 6C4

C3400 0.1uF 20% 10V CERM 402
C3401 10uF 20% 6.3V X5R 603

STANDOFF FOR J3400
CRITICAL
SDF3400
STDOFF-4OD5.6H-1.35-TH
860-0691

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PCI-E MiniCard Connector

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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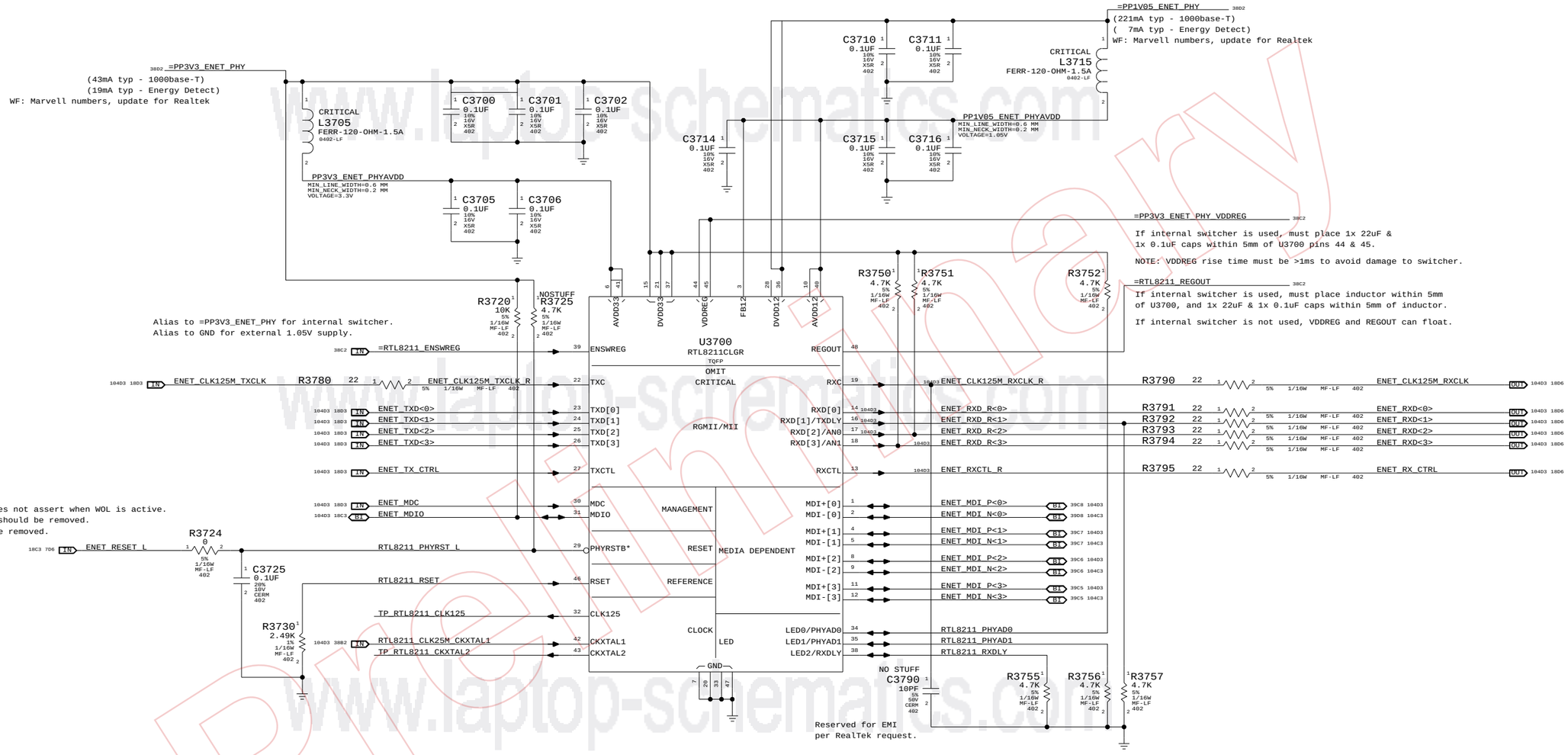
SCALE: NONE	SHT 34 OF 109	



WF: Verify that ENET_RESET_L does not assert when WOL is active.
If true, RC and 0-ohm resistor should be removed.
If false, ENET_RESET_L should be removed.

Configuration Settings:

PHYAD = 01 (PHY Address 00001)
AN[1:0] = 11 (Full auto-negotiation)
RXDLY = 0 (RXCLK transitions with data)
TXDLY = 0 (No TXCLK Delay)

Ethernet PHY (RTL8211CL)

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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SIZE	DRAWING NUMBER	REV.
D	051-7840	10
SCALE: NONE	SHT 37 OF 109	

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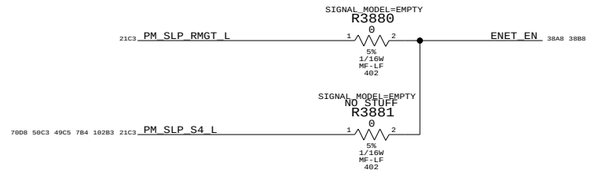
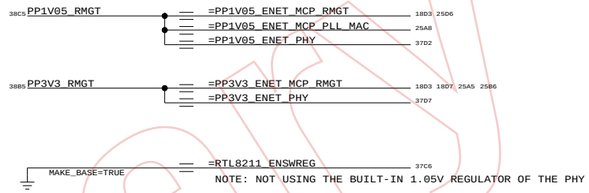
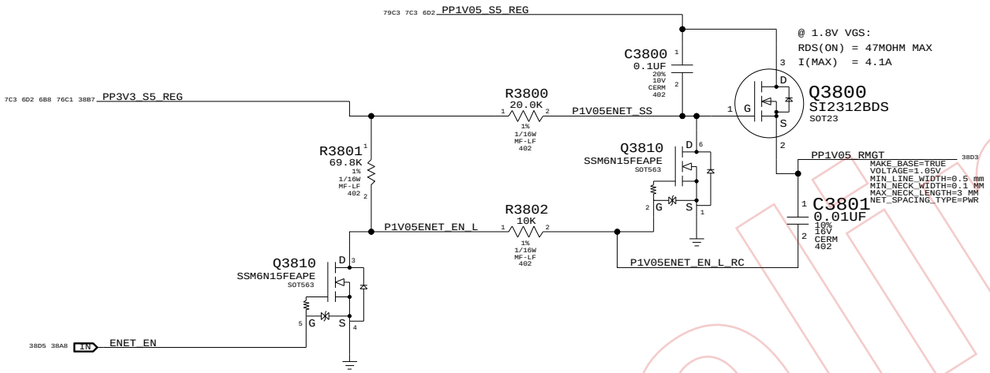
SOURCE SELECT



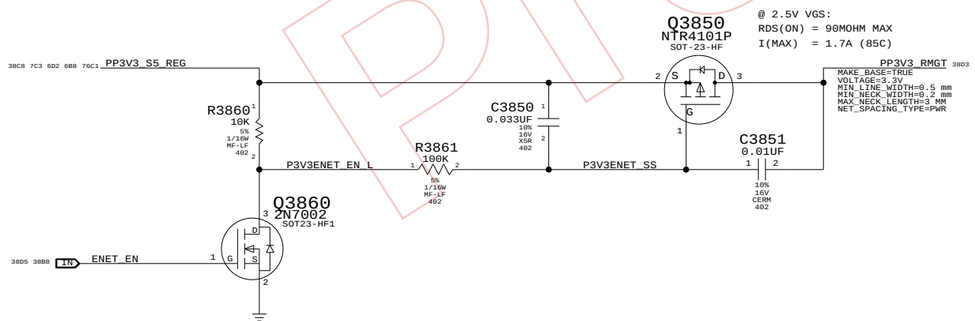
ENET ALIASES



1.05V ENET FET

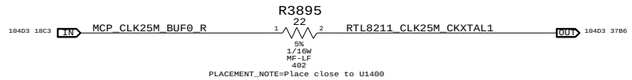


3.3V ENET FET



RTL8211 25MHz Clock

NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered.
Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.



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Ethernet & AirPort Support

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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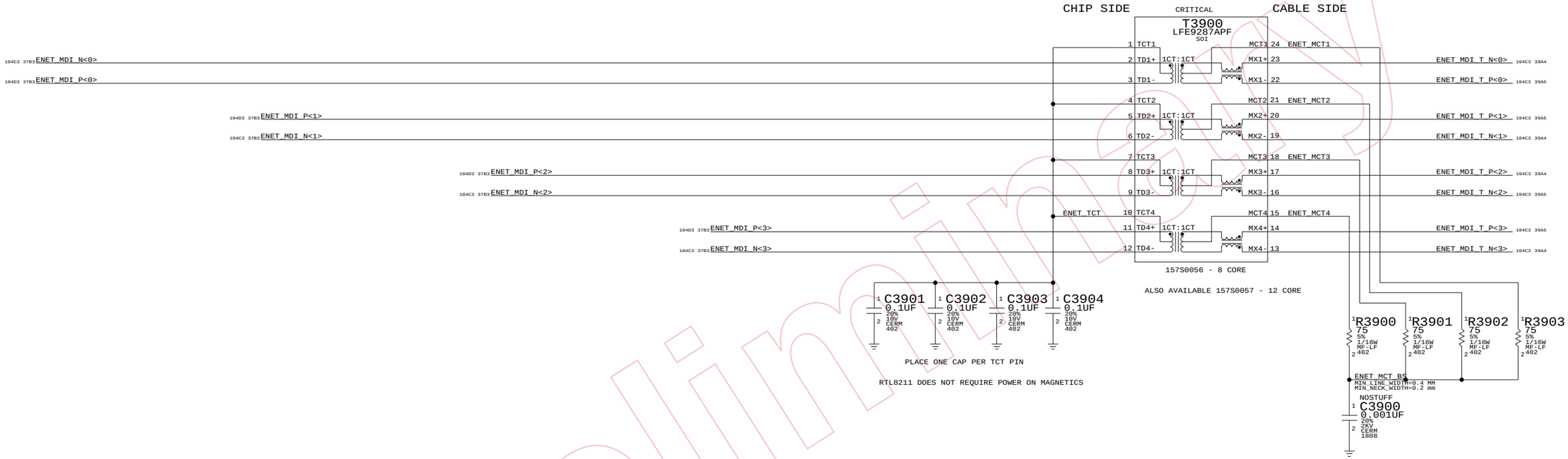
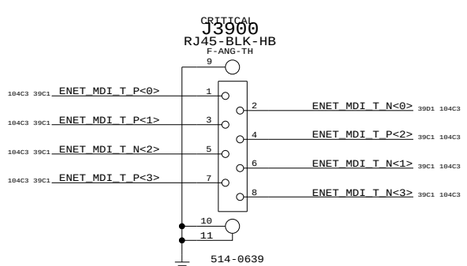
D	051-7840	10
SCALE: NONE	SHT 38 OF 109	

NOTE: DELTA RECOMMENDS CENTER-TAP BE FLOATING WHEN USING REALTEK PHY.



NOTE: BOB SMITH TERMINATION FOR EMC INVESTIGATION.



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ETHERNET CONNECTOR

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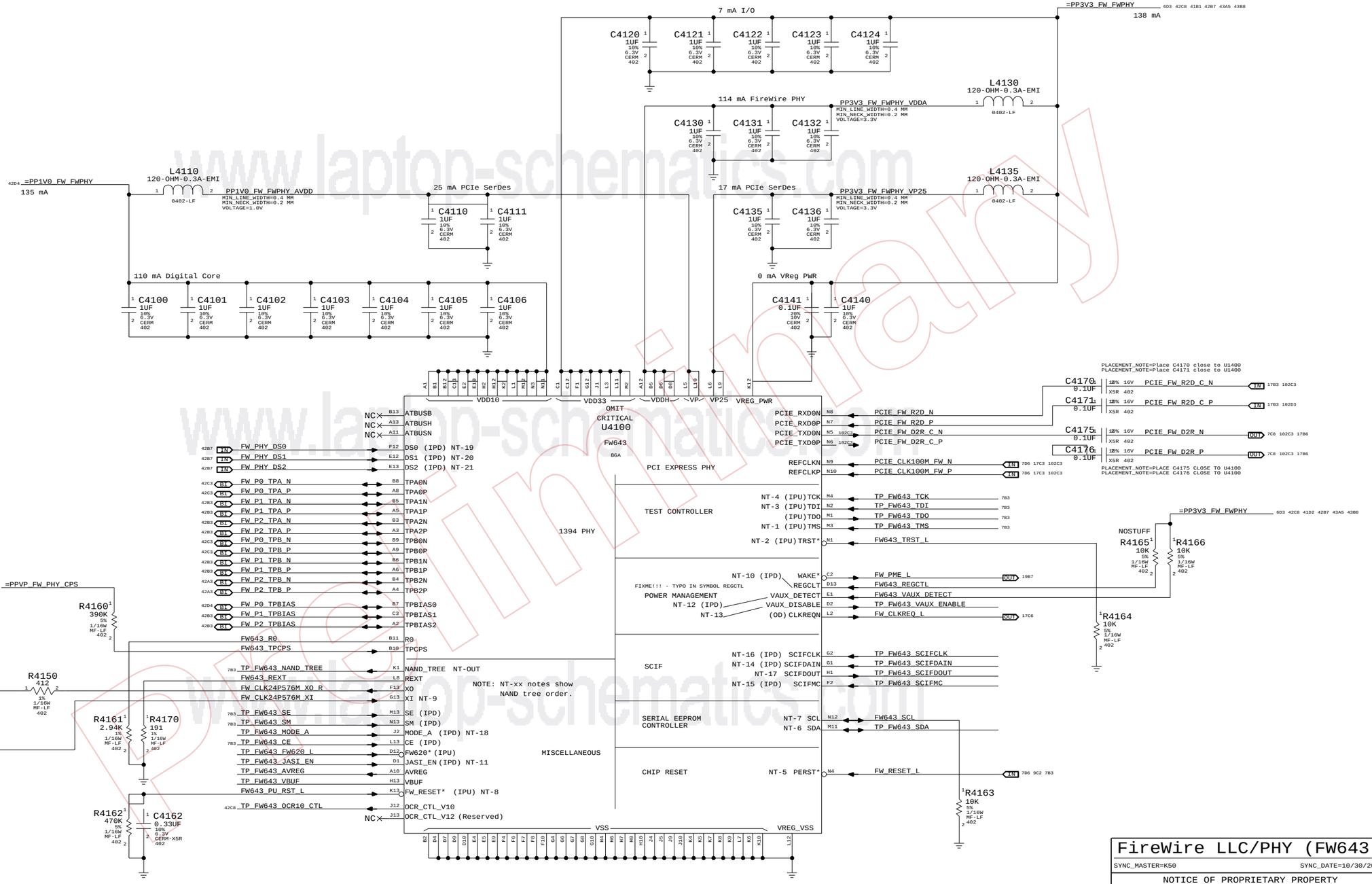
D	051-7840	10

SCALE	SHT	OF
NONE	39	109



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FireWire LLC/PHY (FW643)

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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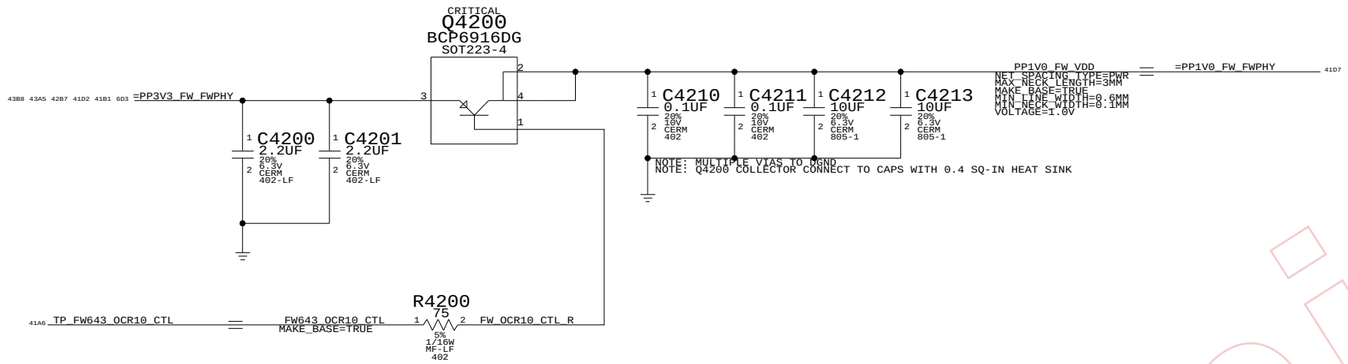
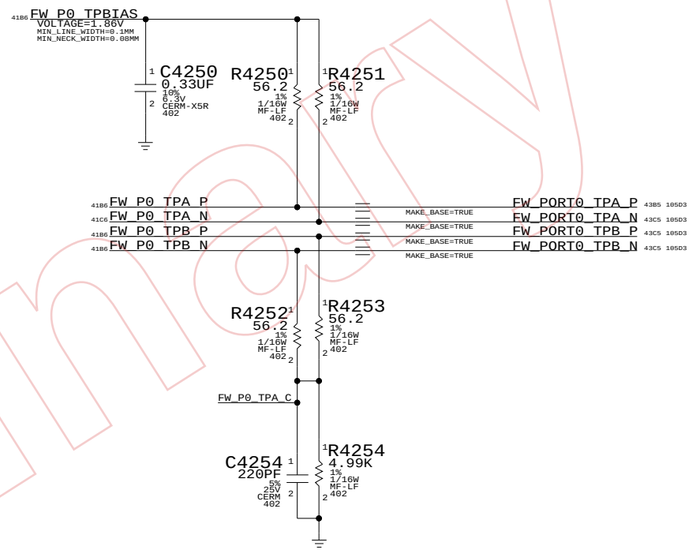
D	051-7840	10
SCALE: NONE	SHT 41 OF 109	

FW643 1.0V GENERATION

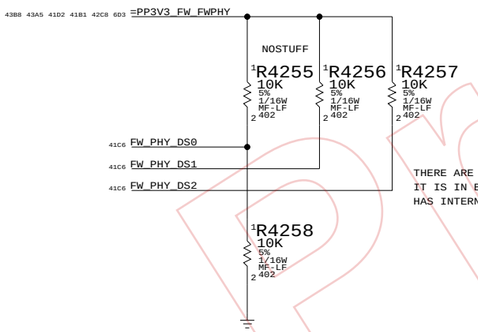


Termination

Place close to FireWire PHY



1394 PHY DATA/STROBE OPTIONS



THERE ARE THREE FIREWIRE PORTS, BUT ONLY ONE IS USED.NO STUFF MEANS THAT IT IS IN BILINGUL MODE PULL-UPS ASSERT/ENABLE DATA STROBE ONLY MODE, FW643 HAS INTERNAL 100K PULL-DOWNS, ONLY PULL-UPS NECESSARY.

2ND & 3RD TPA/TPB PAIR UNUSED

4186 FW_P1_TPBIAS	NC_FW_PORT1_TPBIAS	MAKE_BASE=TRUE, NO_TEST=TRUE
4186 FW_P1_TPA_P	NC_FW_PORT1_TPA_P	MAKE_BASE=TRUE, NO_TEST=TRUE
4186 FW_P1_TPA_N	NC_FW_PORT1_TPA_N	MAKE_BASE=TRUE, NO_TEST=TRUE
4186 FW_P1_TPB_P	NC_FW_PORT1_TPB_P	MAKE_BASE=TRUE, NO_TEST=TRUE
4186 FW_P1_TPB_N	NC_FW_PORT1_TPB_N	MAKE_BASE=TRUE, NO_TEST=TRUE
4186 FW_P2_TPBIAS	NC_FW_PORT2_TPBIAS	MAKE_BASE=TRUE, NO_TEST=TRUE
4186 FW_P2_TPA_P	NC_FW_PORT2_TPA_P	MAKE_BASE=TRUE, NO_TEST=TRUE
4186 FW_P2_TPA_N	NC_FW_PORT2_TPA_N	MAKE_BASE=TRUE, NO_TEST=TRUE
4186 FW_P2_TPB_P	NC_FW_PORT2_TPB_P	MAKE_BASE=TRUE, NO_TEST=TRUE
4186 FW_P2_TPB_N	NC_FW_PORT2_TPB_N	MAKE_BASE=TRUE, NO_TEST=TRUE

NOTE: AGERE'S RECOMMENDATION FOR UNUSED PORTS

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FW: 1394B MISC

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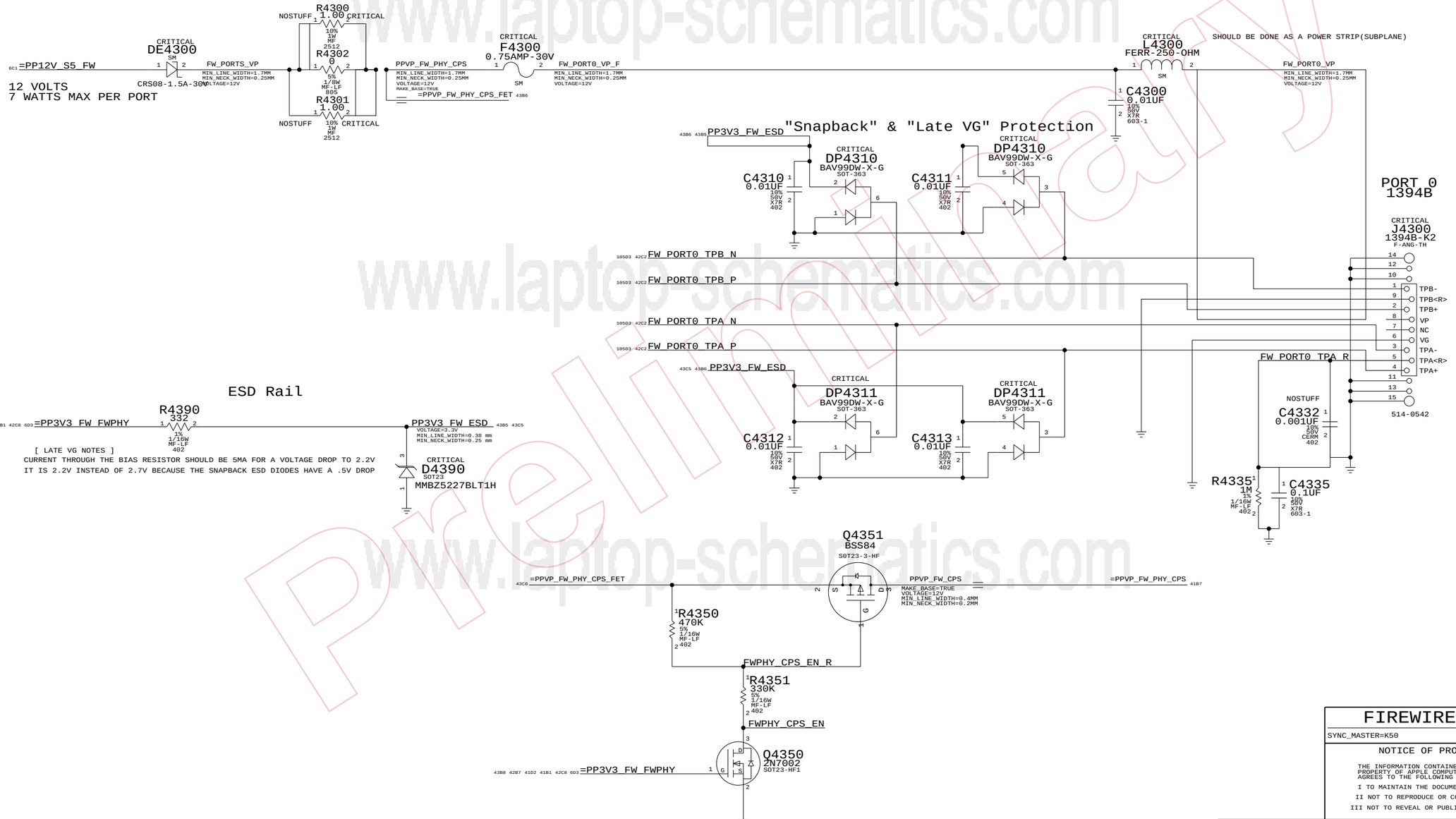
SCALE: NONE SHT 42 OF 109



FIREWIRE CONNECTOR

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D	051-7840	10

SCALE	SHT	OF
NONE	43	109

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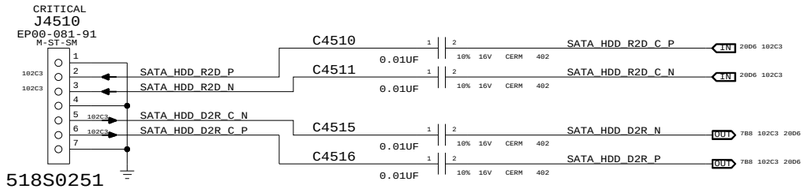
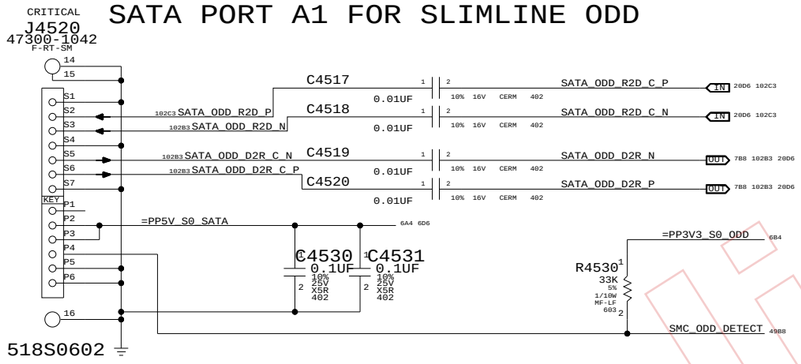
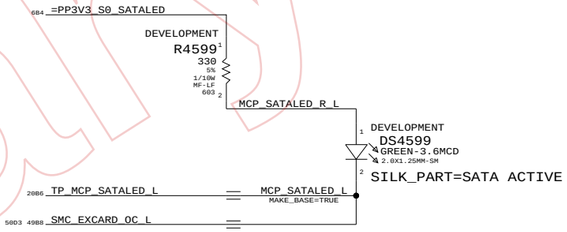
SATA PORT A0 FOR HDD



SATA PORT A1 FOR SLIMLINE ODD



SATA Activity LED



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SATA Connectors

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D	051-7840	10

SCALE	SHT	OF
NONE	45	109

USB PORT 2 AND 3 (C AND D) SHARE OVER-CURRENT WITH PORT 2
PREVIOUSLY, PORT 3 HAD ITS OWN BUT EFI MAPS THAT TO EXPRESSCARD
SEE RDAR://6250424

USB/SMC DEBUG MUX

PORT 3

=PP5V_S3_USB
CRITICAL U4601 TPS2060 MSOP
USB_EXTC_OC_L
R4600 10K 5% 1/16W MF-LF 402
USB_PWR_ENA_L
NOSTUFF CRITICAL C4606 150UF 20% 6.3V POLY-TANT CASE-D2-SM
C4605 0.1UF 20% 10V CERM 402
Q4600 2N7002 SOT23-HF1
PM_EN_USB_PWR
C4621 0.1UF 20% 10V CERM 402
C4631 0.1UF 20% 10V CERM 402
=PP3V3_S5_SMCUSBMUX
C4650 0.1UF 20% 10V CERM 402
CRITICAL U4650 PI3USB102ZLE TQFN
SMC_RX_L
SMC_TX_L
USB_EXTD_P
USB_EXTD_N
USB_DEBUGPRT_EN_L
SEL=0: CHOOSE SMC
SEL=1: CHOOSE USB
NOSTUFF R4651 0 5% 1/16W MF-LF 402
NOSTUFF R4652 0 5% 1/16W MF-LF 402
USB_D_MUXED_N
USB_D_MUXED_P
PP5V_USB2_PORT3 VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
CRITICAL L4630 FERR-250-OHM SM
C4630 0.01UF 20% 16V CERM 402 (PUT CAP ON CONNECTOR SIDE)
PP5V_USB2_PORT3_F VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
CRITICAL L4631 120-OHM-90MA DLP0NS
USB_PORT3_N
USB_PORT3_P
CRITICAL J4630 USB-K50 F-ANG-TH
VDD D- D+ GND VBUS
514-0640
CRITICAL D4630 RCLAMP0502N SLP1210N6
VBUS GND NC IO NC IO

PORT 2

PP5V_USB2_PORT2 VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
CRITICAL L4620 FERR-250-OHM SM
C4620 0.01UF 20% 16V CERM 402 (PUT CAP ON CONNECTOR SIDE)
PP5V_USB2_PORT2_F VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
CRITICAL L4621 120-OHM-90MA DLP0NS
USB_EXTC_N
USB_EXTC_P
USB_PORT2_N
USB_PORT2_P
CRITICAL J4620 USB-K50 F-ANG-TH
514-0640
CRITICAL D4620 RCLAMP0502N SLP1210N6

PORT 1

=PP5V_S3_USB
CRITICAL U4600 TPS2060 MSOP
USB_EXTA_OC_L
USB_EXTB_OC_L
NOSTUFF CRITICAL C4602 150UF 20% 6.3V POLY-TANT CASE-D2-SM
C4601 0.1UF 20% 10V CERM 402
C4603 0.1UF 20% 10V CERM 402
C4611 0.1UF 20% 10V CERM 402
PP5V_USB2_PORT1 VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
CRITICAL L4610 FERR-250-OHM SM
C4610 0.01UF 20% 16V CERM 402 (PUT CAP ON CONNECTOR SIDE)
PP5V_USB2_PORT1_F VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
CRITICAL L4611 120-OHM-90MA DLP0NS
USB_EXTB_N
USB_EXTB_P
USB_PORT1_N
USB_PORT1_P
CRITICAL J4610 USB-K50 F-ANG-TH
514-0640
CRITICAL D4610 RCLAMP0502N SLP1210N6

PORT 0

PP5V_USB2_PORT0 VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
CRITICAL L4600 FERR-250-OHM SM
C4600 0.01UF 20% 16V CERM 402 (PUT CAP ON CONNECTOR SIDE)
PP5V_USB2_PORT0_F VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
CRITICAL L4601 120-OHM-90MA DLP0NS
USB_EXTA_N
USB_EXTA_P
USB_PORT0_N
USB_PORT0_P
CRITICAL J4600 USB-K50 F-ANG-TH
514-0640
CRITICAL D4600 RCLAMP0502N SLP1210N6

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EXTERNAL USB CONNECTORS

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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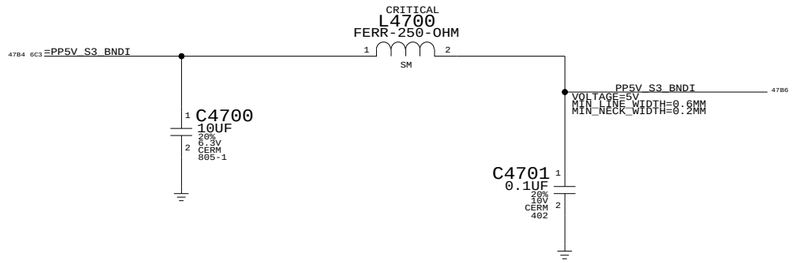
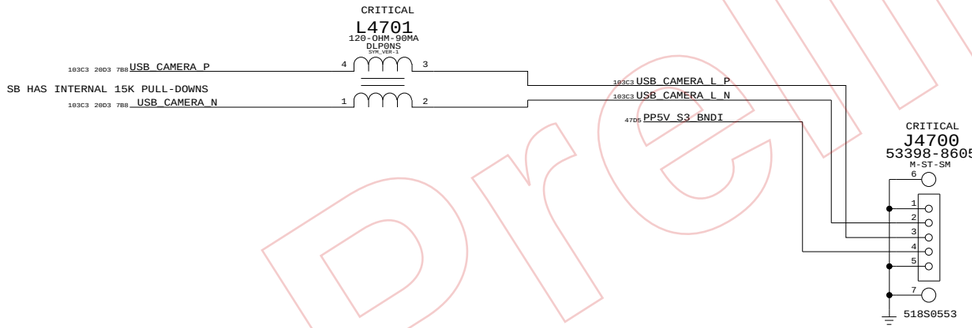
SCALE: NONE
SHT 46 OF 109

CAMERA POWER FILTERING

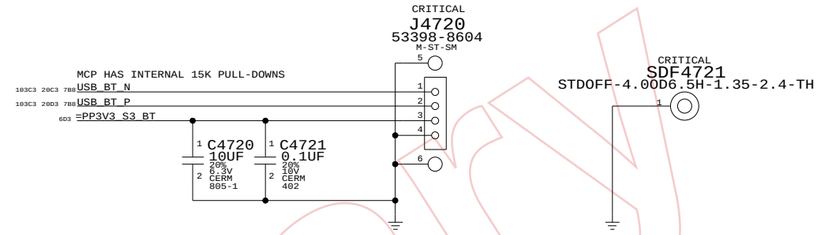


LAYOUT NOTE:
PLACE C4700, C4701 & L4700
NEAR J4700 PINS 4 AND 5 IN THE
ORDER LISTED, AND NOT ON
BOTH SIDES OF THE PIN.

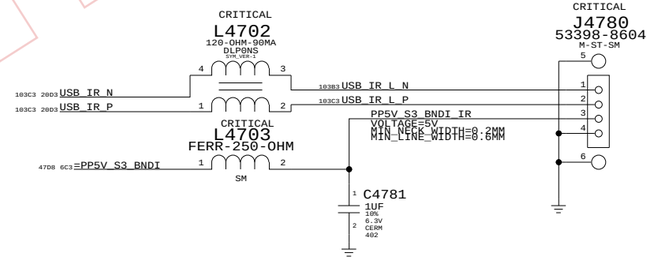
CAMERA CONNECTOR



K37L (BLUETOOTH) CONNECTOR



IR RECEIVER



998-2240
ZH4731
7P5R2P1-NSP

998-2240
ZH4741
7P5R2P1-NSP

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Internal USB Connections

SYNC_MASTER=K51 SYNC_DATE=07/09/2008

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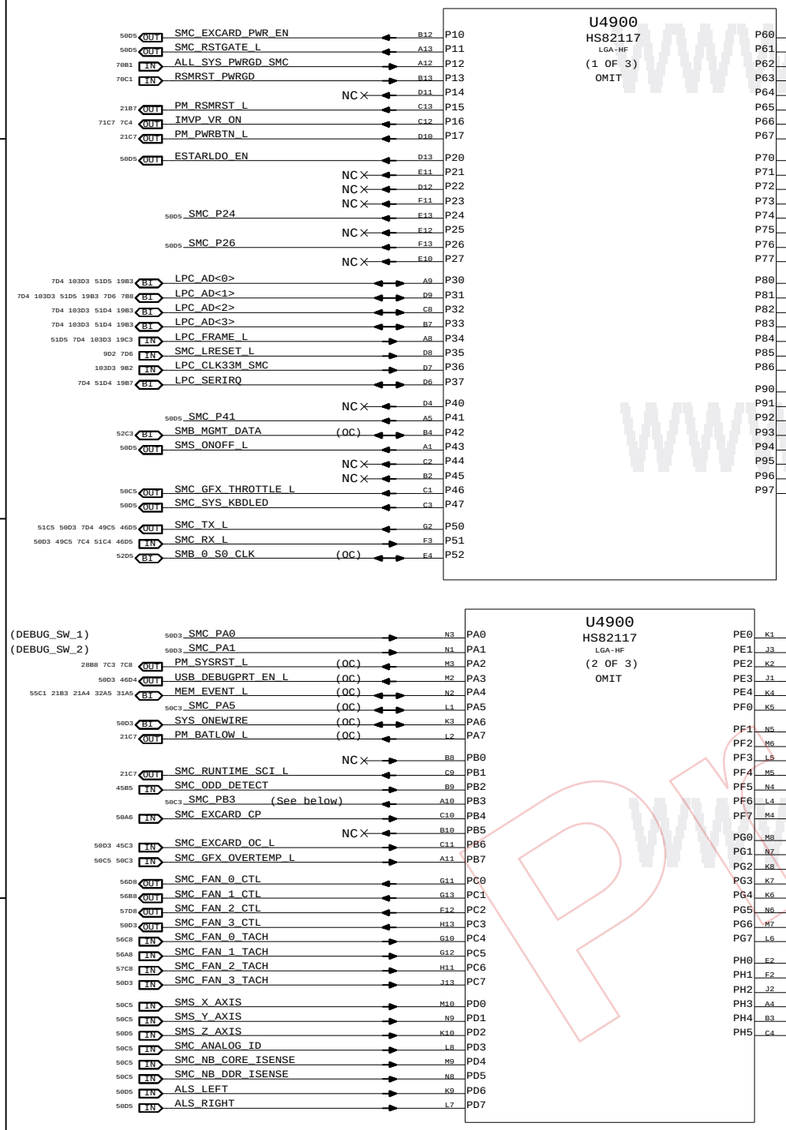
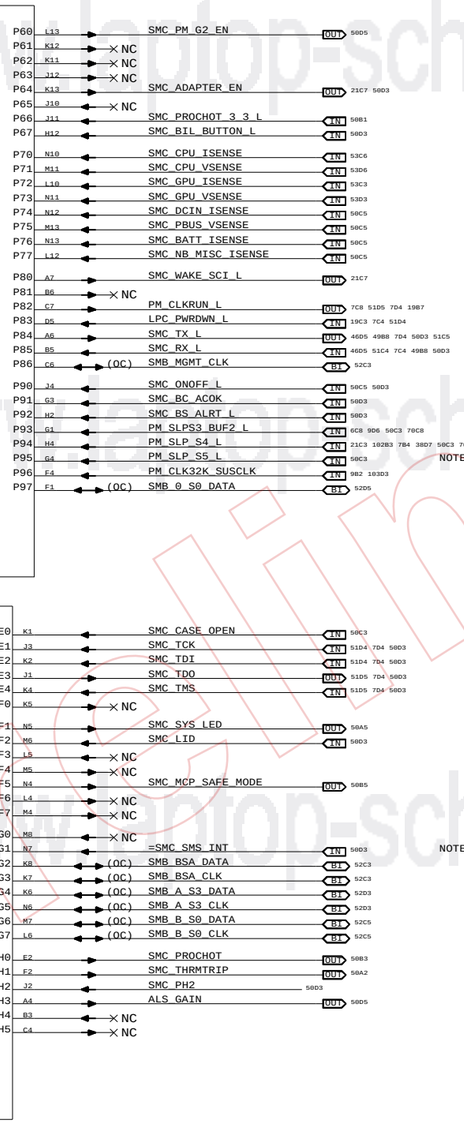
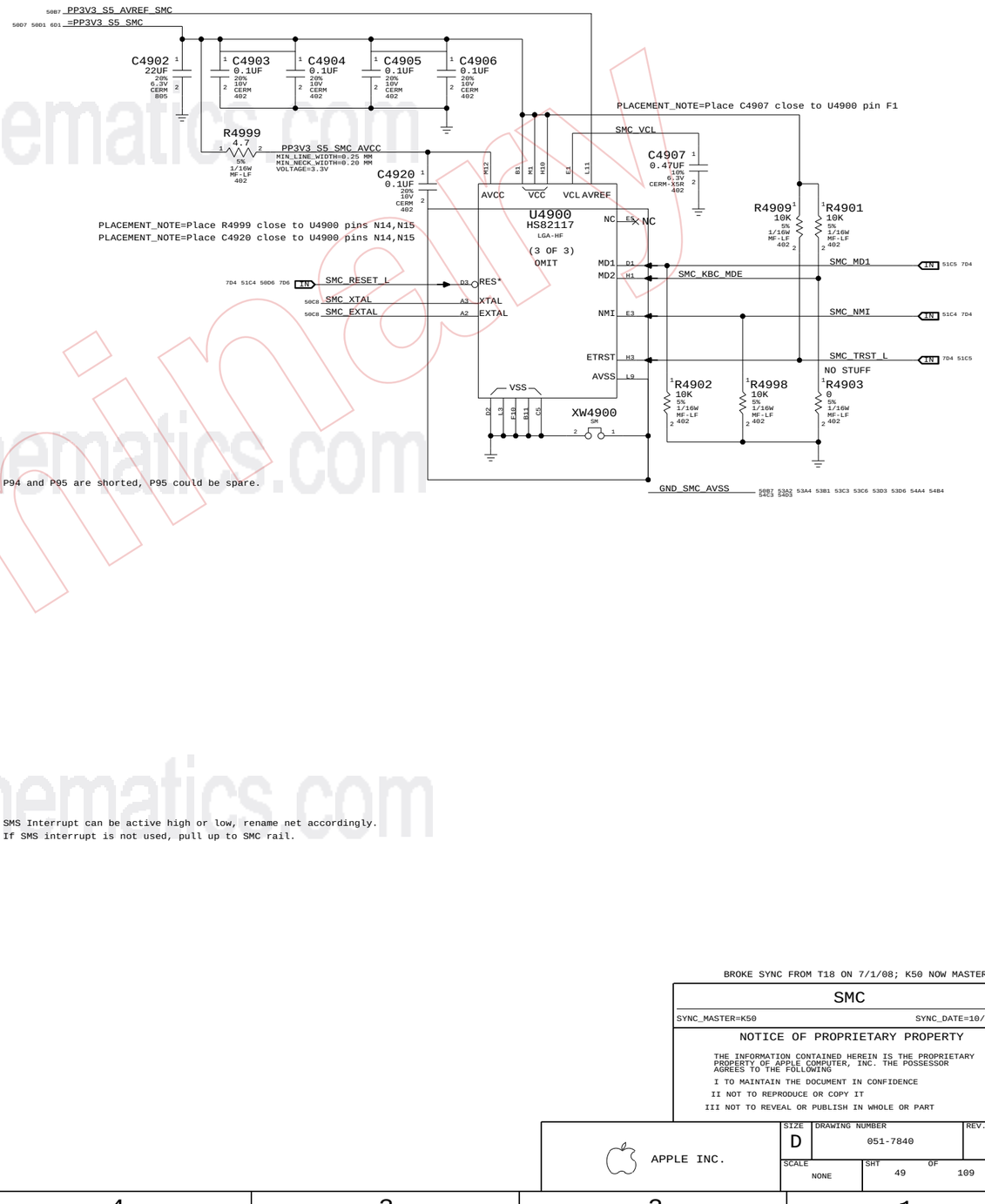
SCALE	SHT	OF
NONE	47	109

NOTE: Unused pins have "SMC_Pxx" names. Unused
pins designed as outputs can be left floating,
those designated as inputs require pull-ups.







NOTE: P94 and P95 are shorted, P95 could be spare.

NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

SMC_PB3:

SMC_IG_THROTTLE_L for MG systems.
Otherwise, TP/NC okay (was ISENSE_CAL_EN)

BROKE SYNC FROM T18 ON 7/1/08; K50 NOW MASTER

SMC

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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SCALE: NONE	SHT 49 OF 109	

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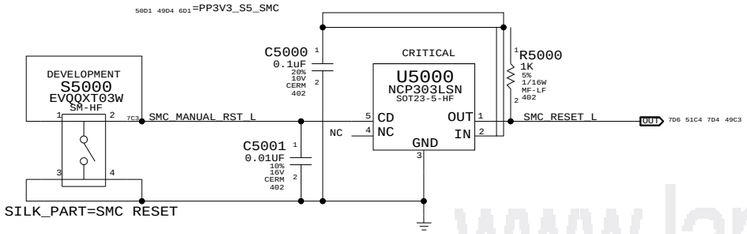
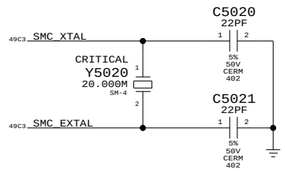
SMC Reset Button / Brownout Detect

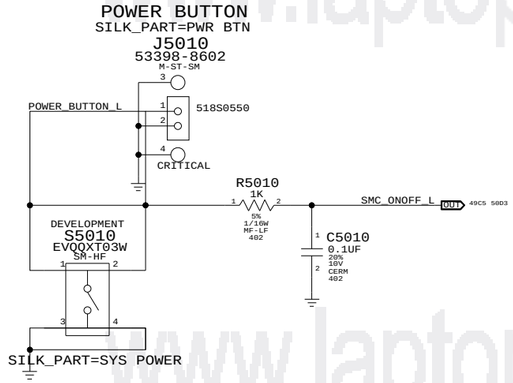


SMC Crystal Circuit



POWER BUTTON

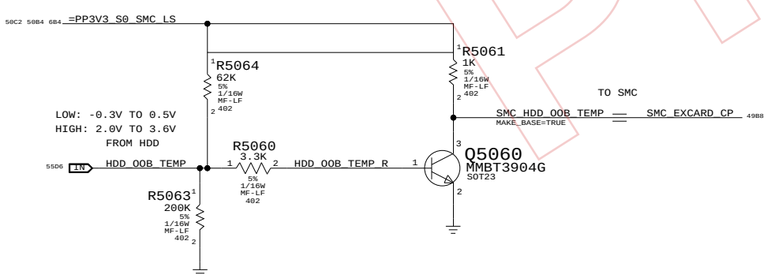
SILK_PART=PWR BTN



SMC AVREF Supply

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1381	353S1278		ALL	Intersil ISL60002-33

HDD OUT OF BAND TEMPERATURE SENSING LEVEL SHIFTING



UNUSED TP/NC ALIASES - PORT D - INTERNAL PULLUPS

49A8 SMS_Z_AXIS	NC_SMS_Z_AXIS	MAKE_BASE=TRUE	NO_TEST=TRUE
49A8 ALS_LEFT	TP_ALS_LEFT	MAKE_BASE=TRUE	
49A8 ALS_RIGHT	TP_ALS_RIGHT	MAKE_BASE=TRUE	

UNUSED TP/NC ALIASES

49A5 ALS_GAIN	NC_ALS_GAIN	MAKE_BASE=TRUE	NO_TEST=TRUE
49D5 SMC_PM_G2_EN	TP_SMC_PM_G2_EN	MAKE_BASE=TRUE	
49C8 SMC_SYS_KBDLED	TP_SMC_SYS_KBDLED	MAKE_BASE=TRUE	
49D8 SMC_EXCARD_PWR_EN	TP_SMC_EXCARD_PWR_EN	MAKE_BASE=TRUE	
49C8 SMS_ONOFF_L	TP_SMS_ONOFF_L	MAKE_BASE=TRUE	
49D8 SMC_RSTGATE_L	TP_SMC_RSTGATE_L	MAKE_BASE=TRUE	
49C8 SMC_P24	TP_SMC_P24	MAKE_BASE=TRUE	
49C8 SMC_P26	TP_SMC_P26	MAKE_BASE=TRUE	
49C8 SMC_P41	TP_SMC_P41	MAKE_BASE=TRUE	
49C8 ESTARLDO_EN	TP_ESTARLDO_EN	MAKE_BASE=TRUE	

ANALOG SENSORS

49C5 SMC_DCIN_ISENSE	SMC_12V_S0_ISENSE	MAKE_BASE=TRUE	53B1
49C5 SMC_PBUS_VSENSE	SMC_12V_S0_VSENSE	MAKE_BASE=TRUE	53B2
49C5 SMC_BATT_ISENSE	SMC_12V_S5_ISENSE	MAKE_BASE=TRUE	53B1
49C5 SMC_NB_MISC_ISENSE	SMC_12V_S5_VSENSE	MAKE_BASE=TRUE	53B4
49A8 SMS_X_AXIS	SMC_1V5_S0_VSENSE	MAKE_BASE=TRUE	54C3
49A8 SMS_Y_AXIS	SMC_MCP_CORE_VSENSE	MAKE_BASE=TRUE	54B4
49A8 SMC_NB_DDR_ISENSE	SMC_1V5_S0_ISENSE	MAKE_BASE=TRUE	54D3
49A8 SMC_NB_CORE_ISENSE	SMC_MCP_CORE_ISENSE	MAKE_BASE=TRUE	54B4

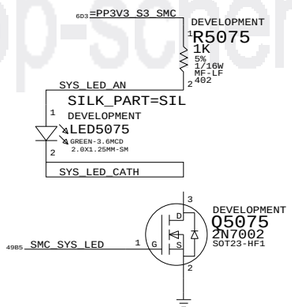
MISC. SIGNAL ALIASES

49A8 SMC_ANALOG_ID	ACDC_TEMP	MAKE_BASE=TRUE	6D6
50C3 49B8 SMC_GFX_OVERTEMP_L	MXM_ALERT_L	MAKE_BASE=TRUE	85B8
49C8 SMC_GFX_THROTTLE_L	MXM_PWR_LEVEL	MAKE_BASE=TRUE	85B8

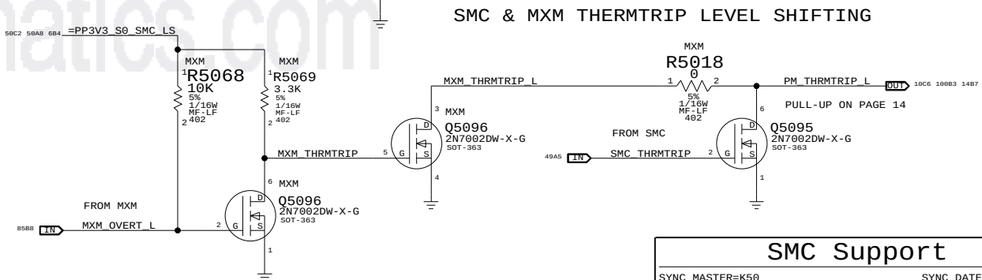
IG
R5020
51
SMC_IG_THROTTLE_L
MAKE_BASE=TRUE
21A4 21B3

R5019
0
49B5 SMC_MCP_SAFE_MODE
MCP_SPKR
21C3
FOR <RDAR://PROBLEM/5925345>

SIL: FOR DEVELOPMENT USE ONLY



SMC & MXM THERMTRIP LEVEL SHIFTING



SMC PROCHOT 3.3V LEVEL SHIFTING

SMC PROCHOT

50D7 49D4 6D1 =PP3V3_S5_SMC

49C5 50C5 SMC_ONOFF_L	R5032	10K	5%	1/16W	MF-LF	402
49B5 SMC_LID	R5033	100K	5%	1/16W	MF-LF	402
49A5 SMC_PH2	R5034	10K	5%	1/16W	MF-LF	402
51C5 7D4 49C5 49B8 46D5 SMC_TX_L	R5035	10K	5%	1/16W	MF-LF	402
49C5 49B8 7C4 51C4 46D5 SMC_RX_L	R5036	100K	5%	1/16W	MF-LF	402
49B8 SYS_ONEWIRE	R5037	2.0K	5%	1/16W	MF-LF	402
49C5 SMC_BS_ALRT_L	R5038	100K	5%	1/16W	MF-LF	402
49B5 7D4 51D5 SMC_TMS	R5039	10K	5%	1/16W	MF-LF	402
7D4 51D5 49B5 SMC_TDO	R5040	10K	5%	1/16W	MF-LF	402
49B5 7D4 51D4 SMC_TDI	R5041	10K	5%	1/16W	MF-LF	402
49B5 7D4 51D4 SMC_TCK	R5042	10K	5%	1/16W	MF-LF	402
49B8 45C3 SMC_EXCARD_OC_L NO STUFF	R5043	10K	5%	1/16W	MF-LF	402
49B8 SMC_PA0	R5096	10K	5%	1/16W	MF-LF	402
49B8 SMC_PA1	R5090	10K	5%	1/16W	MF-LF	402
49C5 SMC_BIL_BUTTON_L	R5092	10K	5%	1/16W	MF-LF	402
49A8 SMC_FAN_3_CTL	R5095	100K	5%	1/16W	MF-LF	402
49A8 SMC_FAN_3_TACH	R5097	100K	5%	1/16W	MF-LF	402
49C5 SMC_BC_ACOK	R5047	10K	5%	1/16W	MF-LF	402
21C7 49D5 SMC_ADAPTER_EN	R5049	10K	5%	1/16W	MF-LF	402
49B8 46D4 USB_DEBUGPRT_EN_L	R5098	10K	5%	1/16W	MF-LF	402
49B5 =SMC_SMS_INT MAKE_BASE=TRUE SMC_SMS_INT	R5091	10K	5%	1/16W	MF-LF	402

54D6 53D5 6B4 =PP3V3_S0_SMC

49B8 SMC_PA5	R5093	10K	5%	1/16W	MF-LF	402
50C5 49B8 SMC_GFX_OVERTEMP_L	R5099	10K	5%	1/16W	MF-LF	402

49B5 SMC_CASE_OPEN	R5046	10K	5%	1/16W	MF-LF	402
70C8 49C5 9D6 6C8 PM_SLPS3_BUF2_L	R5094	100K	5%	1/16W	MF-LF	402
53B8 ISENSE_CAL_EN MAKE_BASE=TRUE	R5088	100K	5%	1/16W	MF-LF	402
49B8 SMC_PB3						
70D8 49C5 38D7 7B4 102B3 21C3 PM_SLP_S4_L MAKE_BASE=TRUE	R5089	100K	5%	1/16W	MF-LF	402
49C5 PM_SLP_S5_L						

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SMC Support

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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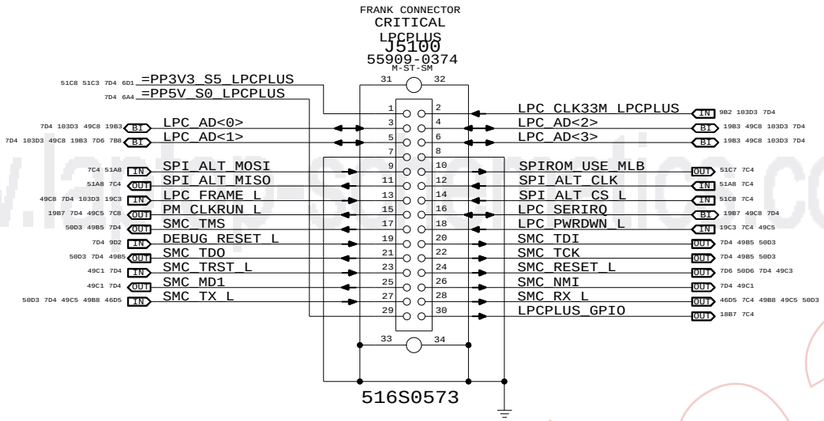
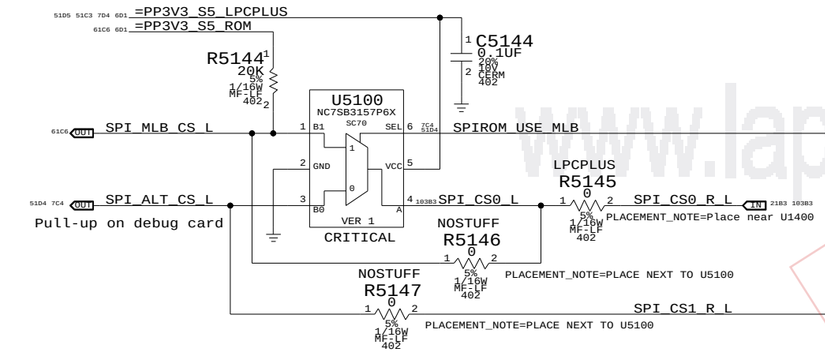
D	051-7840	10
SCALE: NONE	SHT 50 OF 109	

LPC+SPI Connector

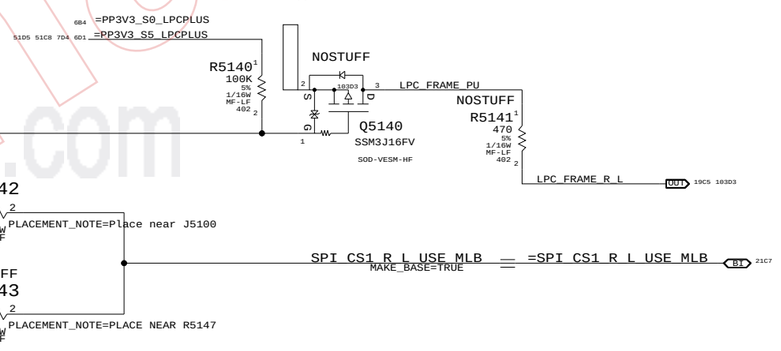


Alternate SPI ROM Support



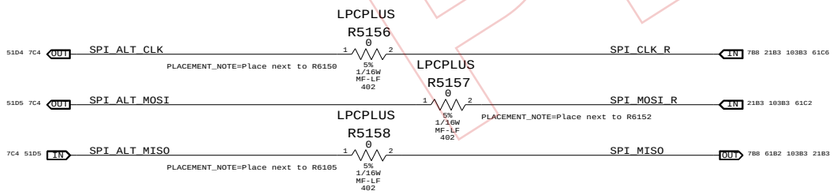
MCP79 Internal SPI MUX Support

Not supported in Rev A01 MCP79 silicon



MCP79 Rev A01 requires external MUX, Rev B01 should support internal MUX

SPI Bus Series Resistance Option



LPC+SPI Debug Connector

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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SIZE	DRAWING NUMBER	REV.
D	051-7840	10
SCALE: NONE	SHT 51 OF 109	

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MCP79 SMBUS "0" CONNECTIONS

52C8 684 =PP3V3_S0_SMBUS

MCP79
U1400
(MASTER)

21C3 706d 106D3 SMBUS_MCP_0_CLK
MAKE_BASE=TRUE

21C3 706d 106D3 SMBUS_MCP_0_DATA
MAKE_BASE=TRUE

R5200[1] 4.7K 5% 1/16W MF-LF 402 [2]

R5201[1] 4.7K 5% 1/16W MF-LF 402 [2]

SMBUS 0 ALSO GOES TO THE XDP CONNECTOR

SO-DIMM "A"
J3100
(Write: 0xA0 Read: 0xA1)

=I2C_SODIMMA_SCL 31A5

=I2C_SODIMMA_SDA 31A5

SO-DIMM "B"
J3200
(WRITE: 0XA2 READ: 0XA3)

=I2C_SODIMMB_SCL 32A5

=I2C_SODIMMB_SDA 32A5

MCP79 SMBUS "1" CONNECTIONS

52D8 684 =PP3V3_S0_SMBUS

MCP79
U1400
(MASTER)

21C3 SMBUS_MCP_1_CLK
MAKE_BASE=TRUE

21C3 SMBUS_MCP_1_DATA
MAKE_BASE=TRUE

R5202[1] 2.2K 5% 1/16W MF-LF 402 [2]

R5203[1] 2.2K 5% 1/16W MF-LF 402 [2]

MIKEY
J9800
(WRITE: 0X72 READ: 0X73)

=I2C_AUDIO_SCL 98C7

=I2C_AUDIO_SDA 98B7

SMC "0" SMBus Connections

684 =PP3V3_S0_SMBUS_SMC_0_S0

SMC
U4900
(MASTER)

49B8 SMB_0_S0_CLK 106D3 SMBUS_SMC_0_S0_SCL
MAKE_BASE=TRUE

49C5 SMB_0_S0_DATA 106D3 SMBUS_SMC_0_S0_SDA
MAKE_BASE=TRUE

R5250[1] 4.7K 5% 1/16W MF-LF 402 [2]

R5251[1] 4.7K 5% 1/16W MF-LF 402 [2]

MXM TEMP
GPU ON CARD - J8400
MV INSIDE (WRITE: 0X9E READ: 0X9F)
MXM CARD (WRITE: 0X98 READ: 0X99)

=SMB_MXM_THRM_SCL 85B8

=SMB_MXM_THRM_SDA 85B8

MCP TEMPS
EMC1403-2: U5535
(WRITE: 0X9A READ: 0X9B)

=SMB_MCP_THRM_SCL 55C2

=SMB_MCP_THRM_SDA 55C2

DIODE1: DIE DIODE2: HEATSINK

SMC "B" SMBus Connections

684 =PP3V3_S0_SMBUS_SMC_B_S0

SMC
U4900
(MASTER)

49A5 SMB_B_S0_CLK 106D3 SMBUS_SMC_B_S0_SCL
MAKE_BASE=TRUE

49A5 SMB_B_S0_DATA 106D3 SMBUS_SMC_B_S0_SDA
MAKE_BASE=TRUE

R5260[1] 4.7K 5% 1/16W MF-LF 402 [2]

R5261[1] 4.7K 5% 1/16W MF-LF 402 [2]

EMC1047-1 HEX DIODE SENSOR

DIODE	FUNCTION
1	ODD TEMP
2	LCD TEMP
3	AMBIENT TEMP
4	CPU HEATSINK
5	MXM HEATSINK
6	HDD TEMP

CPU DIE TEMP
EMC1042-2: U5570
(WRITE: 0X9A READ: 0X9B)

=SMB_CPU_THRM_SCL 55C4

=SMB_CPU_THRM_SDA 55D4

REMOTE TEMPS
EMC1047-1, U5500, SEE TABLE
(WRITE: 0X98 READ: 0X99)

=SMB_REMOTE_TEMP_SCL 55A6

=SMB_REMOTE_TEMP_SDA 55A6

PCI-E MINI CARD
J3400
M35E: NO TEMPERATURE SENSOR
M35B: (WRITE: 0X90 READ: 0X91)

=SMBUS_MINI_SCL 34C3

=SMBUS_MINI_SDA 34C3

DIGITAL LCD TEMP
J5560
TMP275: U1
(WRITE: 0X94 READ: 0X95)

=SMB_LCD_TEMP_SCL 55A4

=SMB_LCD_TEMP_SDA 55A4

SMC "A" SMBus Connections

NOTE: SMC RMT BUS REMAINS POWERED AND MAY BE ACTIVE IN S3 STATE

6D3 =PP3V3_S3_SMBUS_SMC_A_S3

SMC
U4900
(MASTER)

49A5 SMB_A_S3_CLK 106D3 SMBUS_SMC_A_S3_SCL
MAKE_BASE=TRUE

49A5 SMB_A_S3_DATA 106D3 SMBUS_SMC_A_S3_SDA
MAKE_BASE=TRUE

R5270[1] 100K 5% 1/16W MF-LF 402 [2]

R5271[1] 100K 5% 1/16W MF-LF 402 [2]

UNUSED SMC "BATTERY A" SMBUS CONNECTIONS

6D1 =PP3V3_S5_SMBUS_SMC_BSA

SMC
U4900
(MASTER)

49B5 SMB_BSA_CLK 106D3 SMBUS_SMC_BSA_SCL
MAKE_BASE=TRUE

49B5 SMB_BSA_DATA 106D3 SMBUS_SMC_BSA_SDA
MAKE_BASE=TRUE

R5280[1] 100K 5% 1/16W MF-LF 402 [2]

R5281[1] 100K 5% 1/16W MF-LF 402 [2]

SMC "MANAGEMENT" SMBUS CONNECTIONS

684 =PP3V3_S0_SMBUS_SMC_MGMT

SMC
U4900
(MASTER)

49C5 SMB_MGMT_CLK 106D3 SMBUS_SMC_MGMT_SCL
MAKE_BASE=TRUE

49C5 SMB_MGMT_DATA 106D3 SMBUS_SMC_MGMT_SDA
MAKE_BASE=TRUE

R5290[1] 4.7K 5% 1/16W MF-LF 402 [2]

R5291[1] 4.7K 5% 1/16W MF-LF 402 [2]

VREF DAC
U2900
(Write: 0x98 Read: 0x99)

=I2C_VREFDACS_SCL 29C7

=I2C_VREFDACS_SDA 29C7

MARGINGING CONTROL
U2901
(WRITE: 0X30 READ: 0X31)

=I2C_PCA9557D_SCL 29A8

=I2C_PCA9557D_SDA 29A8

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SMBUS CONNECTIONS

SYNC_MASTER=DEREK SYNC_DATE=10/15/2008

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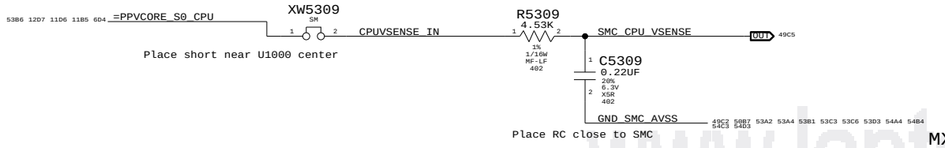
D	051-7840	10

SCALE	SHT	OF
NONE	52	109

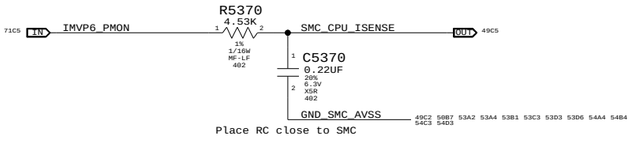
CPU POWER SENSE CALIBRATION CIRCUIT

Switches in fixed load on power supplies to calibrate current sense circuits

CPU Voltage Sense / Filter



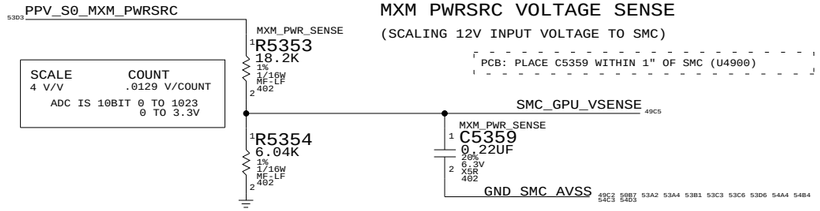
CPU SUPPLY POWER SENSE FILTER



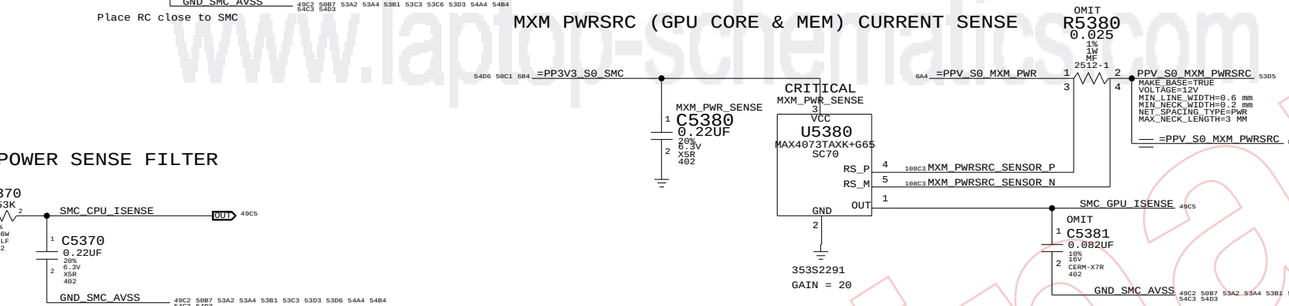
PCPU = VPMON / (17.5 * .0021)

MXM PWRSRC VOLTAGE SENSE

(SCALING 12V INPUT VOLTAGE TO SMC)



MXM PWRSRC (GPU CORE & MEM) CURRENT SENSE



K50 SET FOR APPROX 2V AT 4A ON PWRSRC

SCALE	COUNT
2 A/V	.0064453 A/COUNT

ADC IS 10BIT 0 TO 1023
0 TO 3.3V

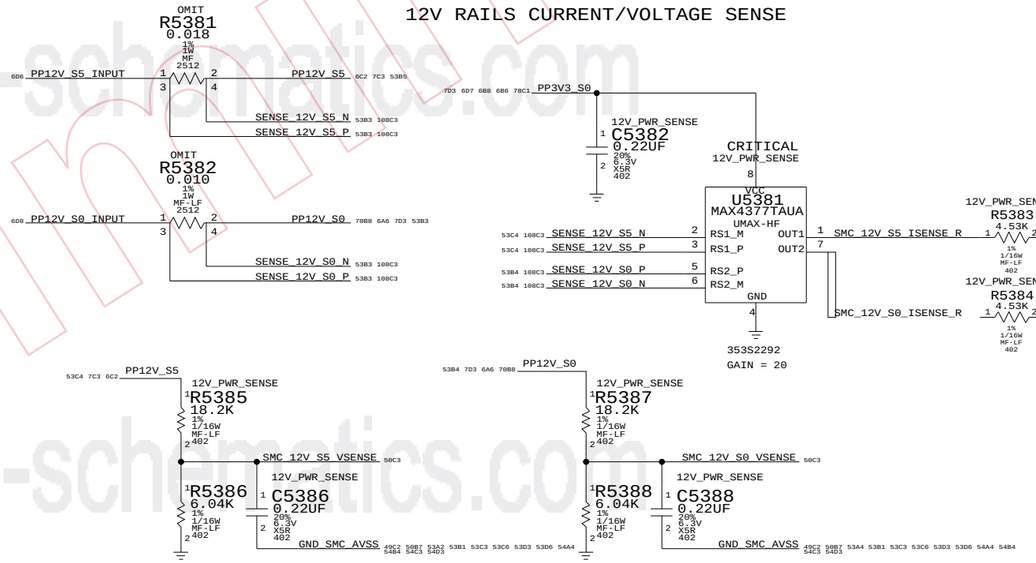
K51 SET FOR APPROX 1.98V AT 5.5A ON PWRSRC

SCALE	COUNT
2.778 A/V	.0087518 A/COUNT

ADC IS 10BIT 0 TO 1023
0 TO 3.3V

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
107S0063	1	25 MILLIOHM	R5380	CRITICAL	K50_BETTER
107S0111	1	18 MILLIOHM	R5380	CRITICAL	24_INCH_MXM
132S0242	1	CAP,0.082UF,402	C5381	CRITICAL	MXM_PWR_SENSE
116S0090	1	RES,10KOHM,5%,402	C5381	CRITICAL	IG

12V RAILS CURRENT/VOLTAGE SENSE

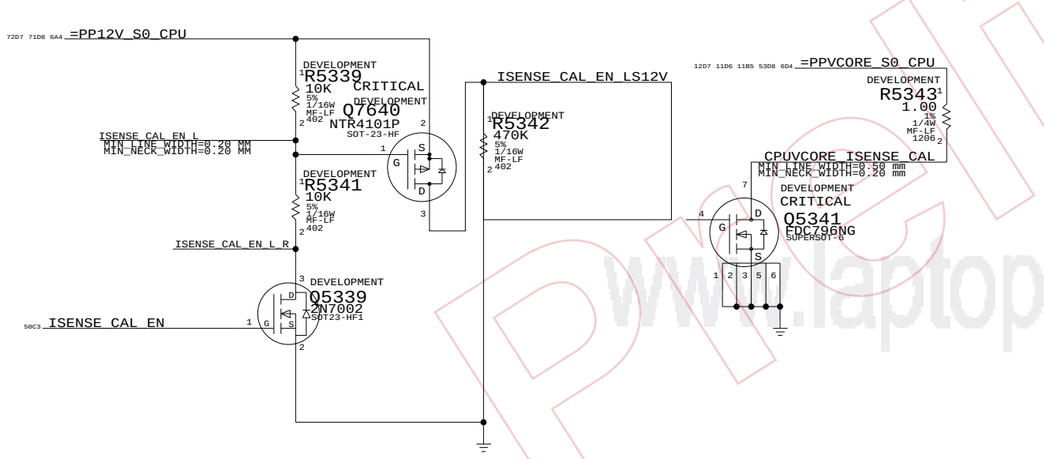


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION	RANGE
107S0069	1	10 MILLIOHM	R5382	CRITICAL	K50_BETTER	10A
107S0112	1	8 MILLIOHM	R5382	CRITICAL	24_INCH_MXM	12.5A
107S0070	2	RES,0 OHM,2512	R5381,R5382	CRITICAL	IG	
107S0111	1	18 MILLIOHM	R5381	CRITICAL	12V_PWR_SENSE	5.5A
116S0090	2	RES,10K0HM,5%,402	C5383,C5384		IG	
132S0080	2	CAP,0.22UF,20%,6.3V,X5R,402	C5383,C5384		12V_PWR_SENSE	

12V_PWR_SENSE SHOULD BE STUFFED FOR MXM CONFIGS
IG CONFIGS WILL NOT HAVE THE SENSORS, SO CAPS FROM THE RC FILTER BECOME RESISTORS TO GROUND (SO SMC READS 0)

IG CONFIGS DO NOT NEED 12V POWER SENSE BECAUSE THE CONFIGURATION DOES NOT DRAW CURRENT WHICH APPROACHES THE ACDC SPEC

CPU Power Sense Calibration Circuit



Current & Voltage Sensing
SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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D	051-7840	10

SCALE NONE SHT 53 OF 109

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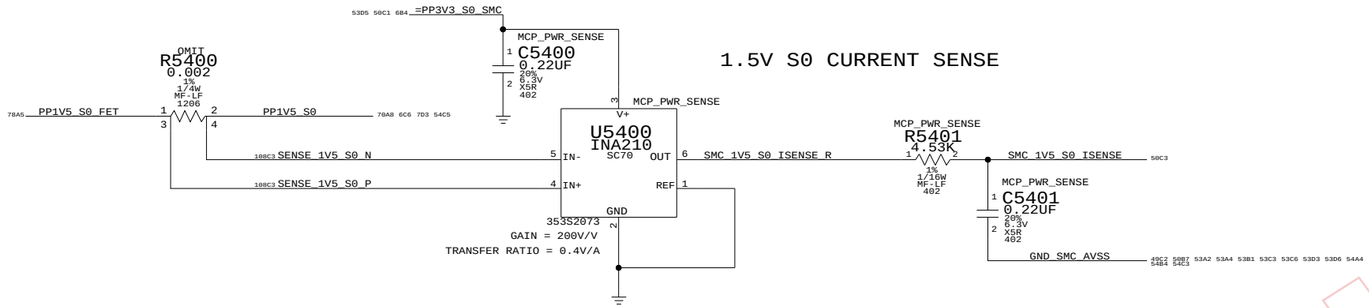
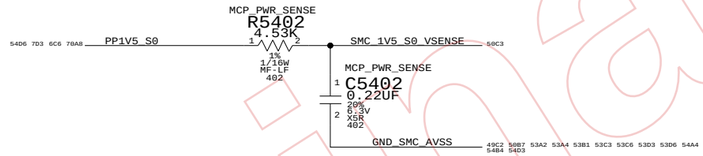
1.5V S0 CURRENT SENSE

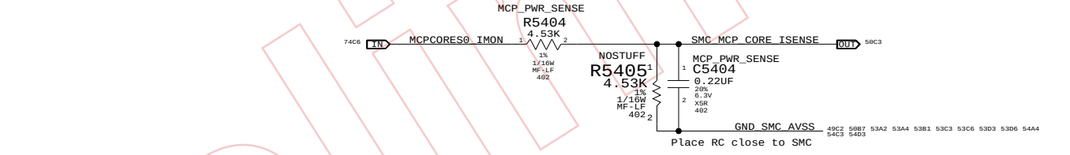


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
104S0018	1	RES,2 MILLIOHM,1206	R5400	CRITICAL	MCP_PWR_SENSE
101S0414	1	RES,0 OHM,1206,20MILLIOHM MAX	R5400	CRITICAL	PRODUCTION

1.5V S0 VOLTAGE SENSE

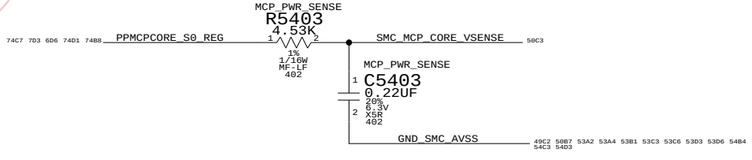


MCP CORE CURRENT SENSE



SCALE IS 0.116 V/A

MCP CORE VOLTAGE SENSE



Preliminary

MCP CURRENT AND VOLTAGE SENSE

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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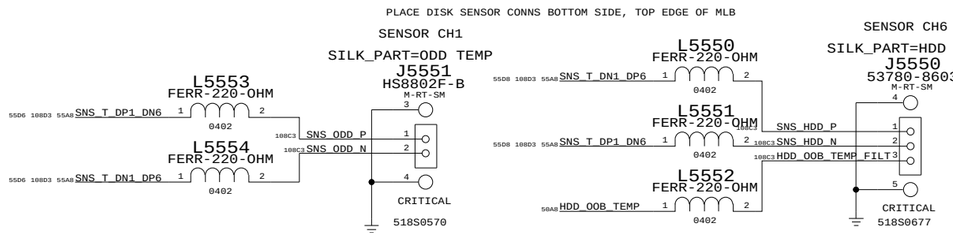
D	051-7840	10
SCALE: NONE	SHT 54 OF 109	

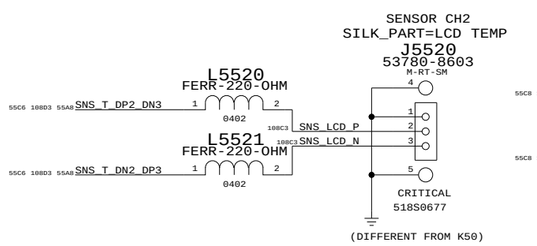
REMOTE THERMAL SENSORS

HEATSINKS, AMBIENT, PANEL AND DISKS

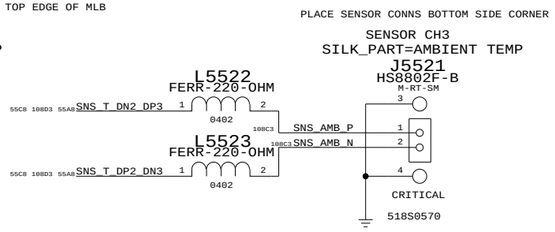
PLACE DISK SENSOR CONNS BOTTOM SIDE, TOP EDGE OF MLB



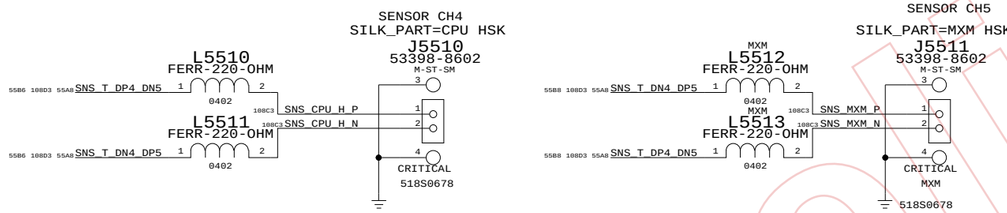
PLACE ANALOG LCD TEMP CONN BOTTOM SIDE, TOP EDGE OF MLB



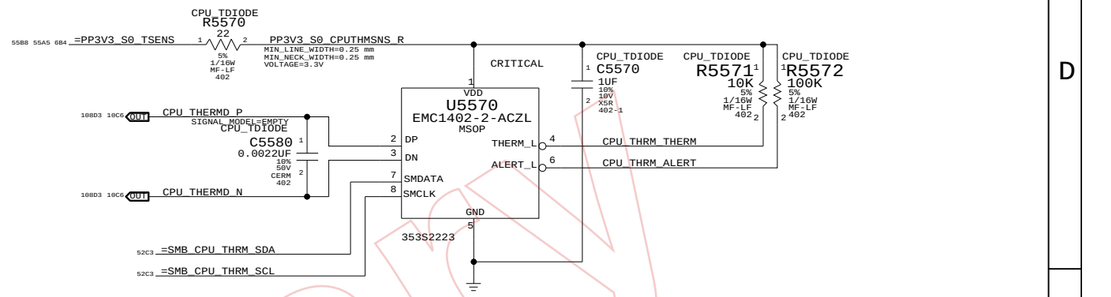
PLACE SENSOR CONNS BOTTOM SIDE CORNER



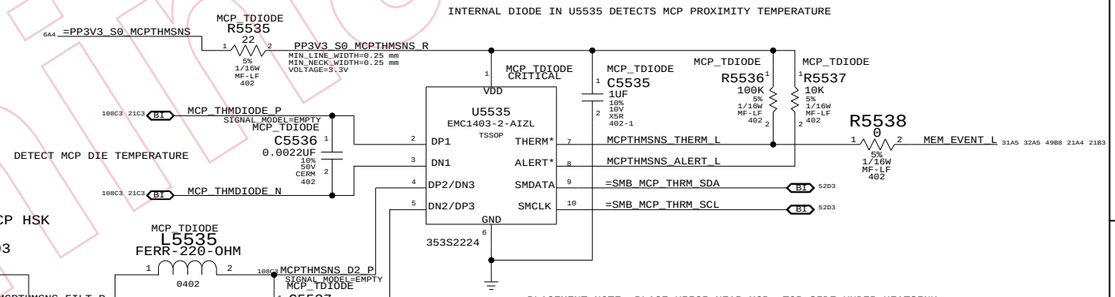
PLACE HSK SENSOR CONN. TOP SIDE NEAR MXM OR CPU



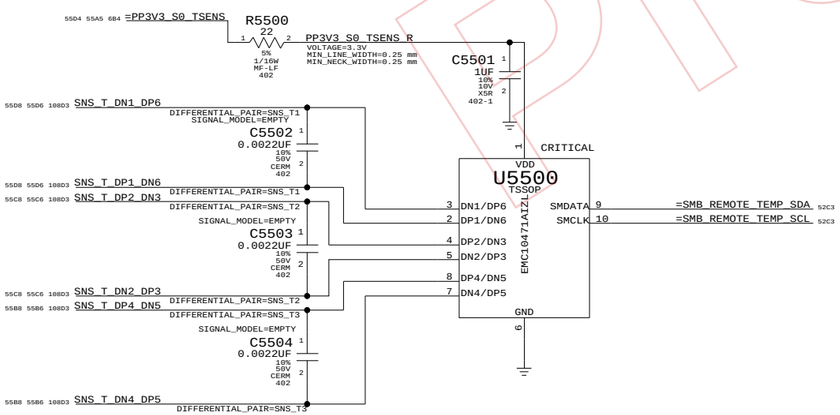
CPU T-Diode Thermal Sensor



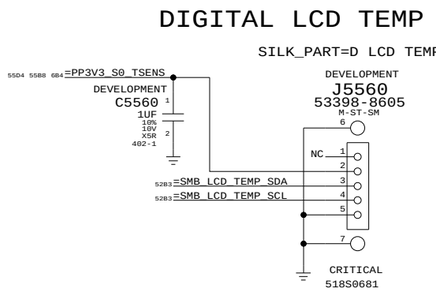
MCP T-Diode Thermal Sensor



REMOTE THERMAL SENSORS (HEATSINKS AND DISKS)



DIGITAL LCD TEMP SENSOR



BROKE SYNC FROM K50 ON 7/9

Thermal Sensors

SYNC_MASTER=DEREK SYNC_DATE=10/15/2008

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SCALE: NONE	SHT 55 OF 109	

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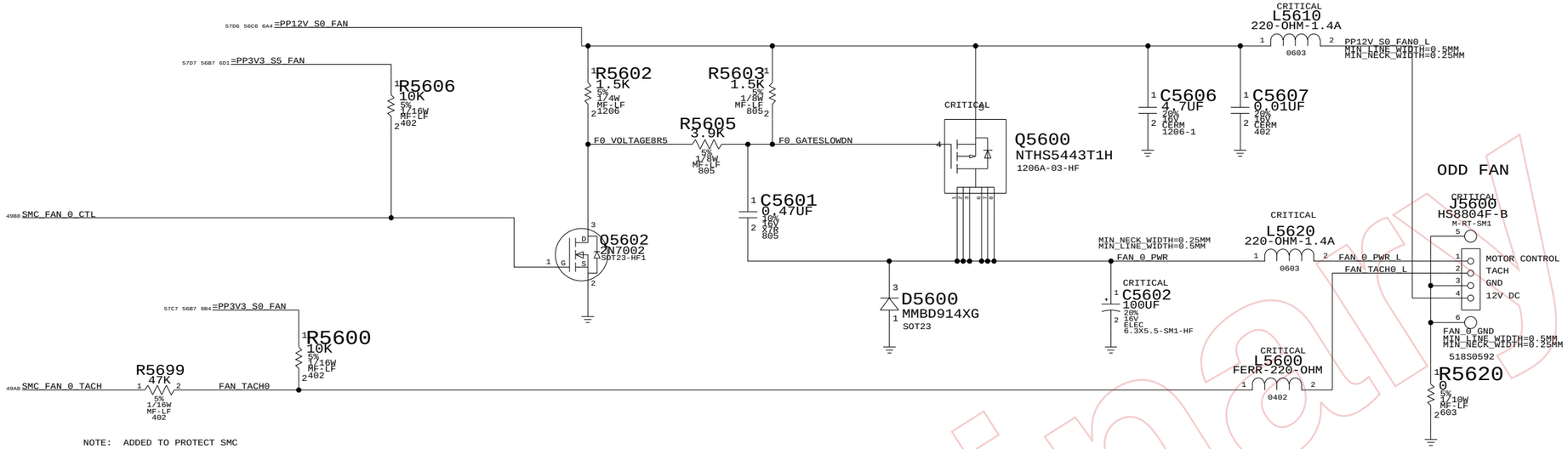
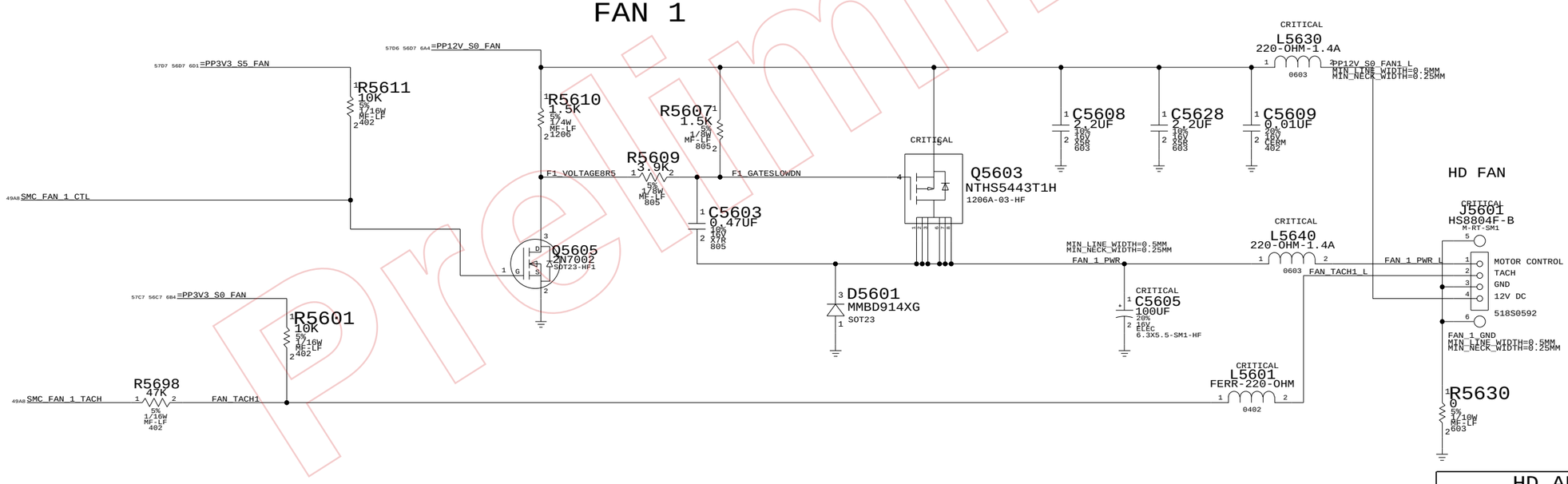
FAN 0



NOTE: ADDED TO PROTECT SMC

FAN 1



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HD AND OD FAN

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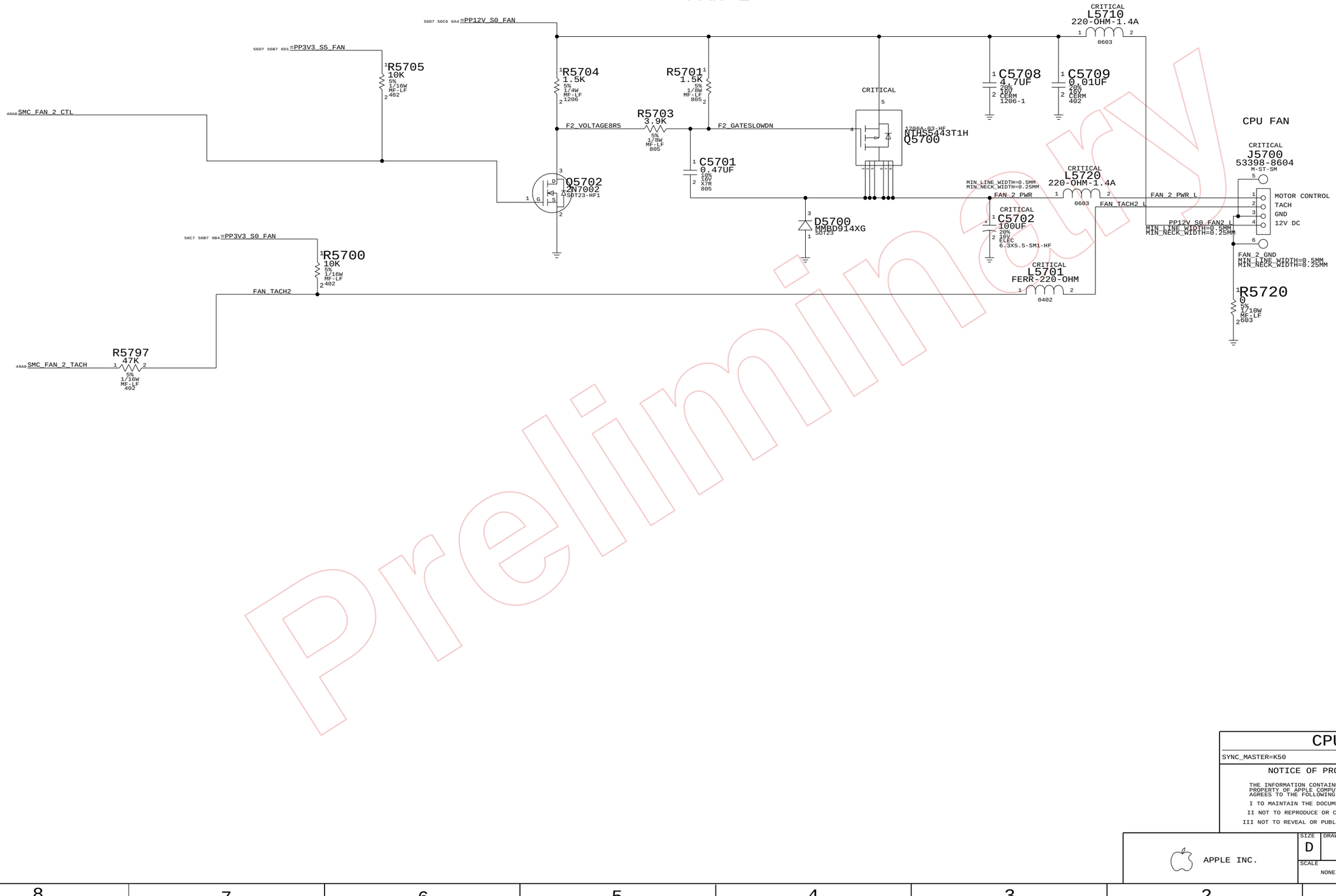
FAN 2



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CPU FAN

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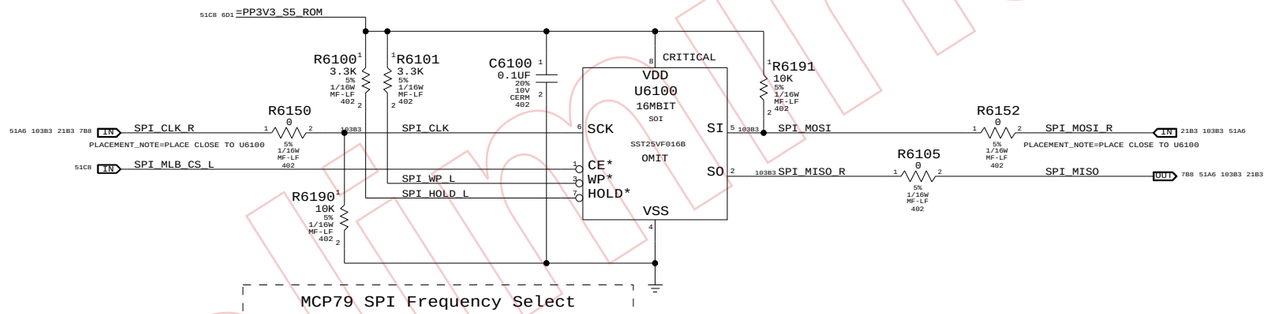
NONE	57	109



MCP79 SPI Frequency Select

Frequency	SPI_MOSI	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

NOTE: MCP79 only issues 'READ' (0x03) commands not 'READ_FAST' (0x0B). Limits SPI bus frequency and part selection.

SST25VF016B max speed for READ command is 25MHz.

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SPI ROM

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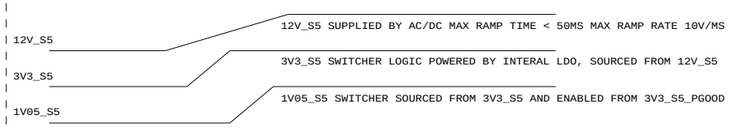
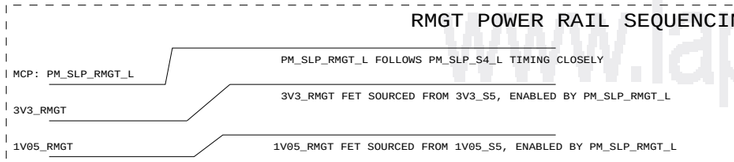
SCALE: NONE SHT 61 OF 109

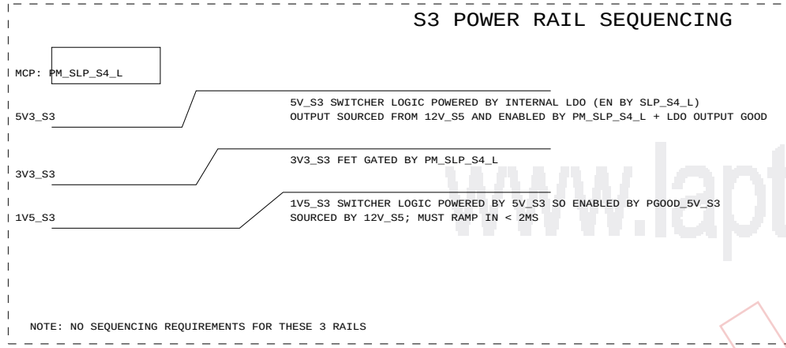
S5 POWER RAIL SEQUENCING



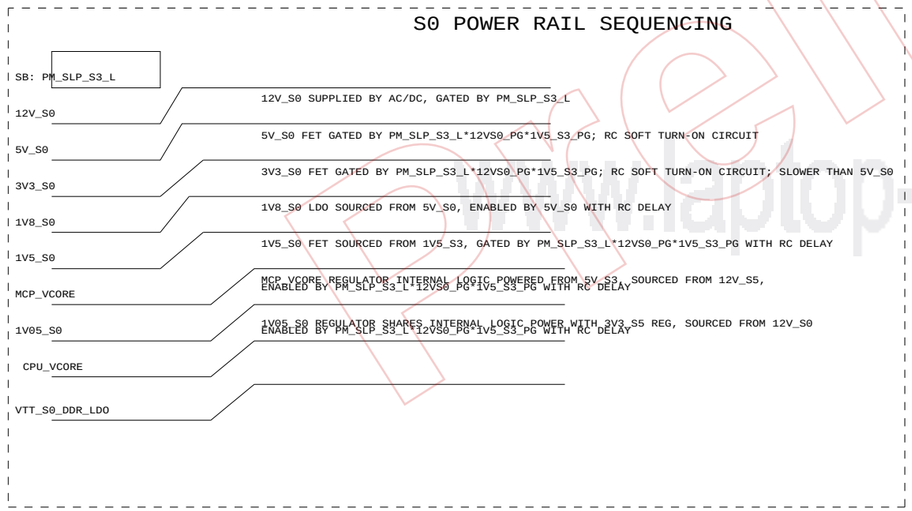
RMGT POWER RAIL SEQUENCING



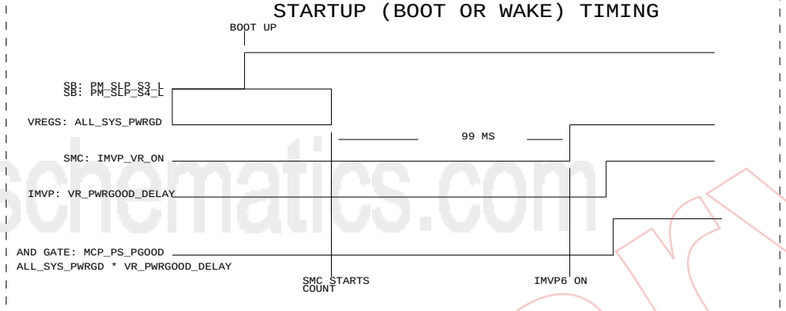
S3 POWER RAIL SEQUENCING



S0 POWER RAIL SEQUENCING



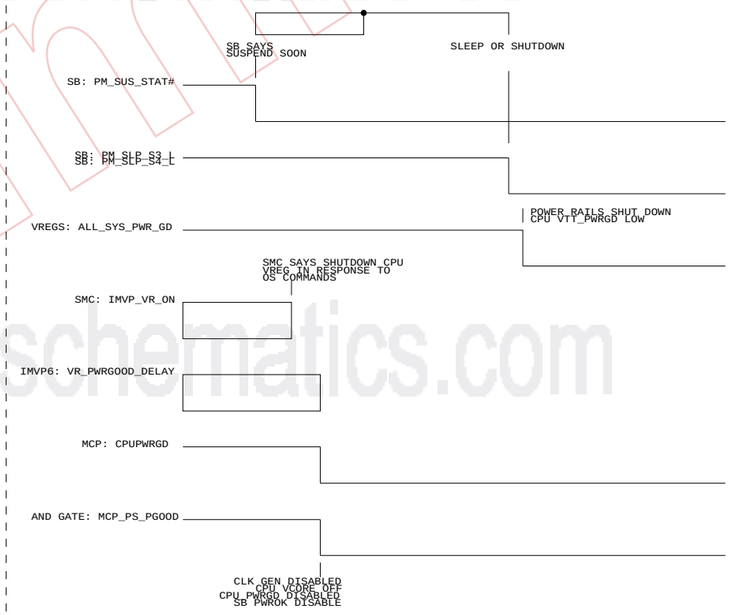
STARTUP (BOOT OR WAKE) TIMING



State	Manageability	SMC_PM_G2_ENABLE	PM_S4_STATE_L	PM_SLP_S3_L	PM_SLP_S4_L	PM_SLP_M_L
Run (S0/M0)	N/A	1	1	1	1	1
Sleep (S3/M1)	On	1	1	0	1	1
Soft-Off (S5/M1)	On	1	0	0	1	1
Sleep (S3/M-Off)	Off	1	1	0	1	0
Soft-Off (S5/M-Off)	Off	1	0	0	0	0
Battery Off (G3Hot)	N/A	0	0	0	0	0

SHUT DOWN (SHUTDOWN OR SLEEP) TIMING

POWER RAILS ON DURING THIS TIME



POWER SEQUENCING BLOCK DIAGRAM

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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NONE	69	109

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Power Control Signals

3.3V,5V S3 enable

FROM MCP (6)

50C3 49C5 38D7 7B4 102B3 21C3 IN PM_SLP_S4_L

(PM_S4_STATE_L) MAKE_BASE=TRUE

=P3V3S3_EN OUT 78D4 Enable FET

=5VREG_EN OUT 73C6 ENABLE REGULATOR

78B7 6C9 =PP5V_S3_PWRCTL

R7072 100K 5% 1/16W MF-LF 402

9A7 PGOOD_5V_S3 MAKE_BASE=TRUE

=DDRREG_EN OUT 75C8 Enable regulator

70C1 70B3 70B1 70A3 6D1 =PP3V3_S5_PWRCTL

C7058 0.1UF 20% 10V CERM 402

R7040 100K 5% 1/16W MF-LF 402

FROM COMPARATOR

70B4 PGOOD_1V5_S3

FROM COMPARATOR

70B4 PGOOD_12V_S0

S0_RDY MAKE_BASE=TRUE

TC7SZ08AFEAPE SOT665

U7059

49C5 9D6 6C8 50C3 IN PM_SLPS3_BUF2_L

(PM_SLP_S3_L) MAKE_BASE=TRUE

From SMC (6)

4 (PM_SLP_S3_L_BUF)

PM_SLP_S3_L_AND_S0_RDY MAKE_BASE=TRUE

=P5VS0_EN OUT 78D7 Enable FET

=P3V3S0_EN OUT 78C4 Enable FET

R7080 30K 5% 1/16W MF-LF 402

R7081 43K 5% 1/16W MF-LF 402

R7082 10K 5% 1/16W MF-LF 402

MCPDDR_EN MAKE_BASE=TRUE

=MCPDDR_EN OUT 78A7 Enable FET DELAY OF ~15MS FROM PM_SLP_S3_L

CPUVTTS0_EN MAKE_BASE=TRUE

=1V05S0_EN OUT 76B7 Enable regulator DELAY OF ~18MS FROM PM_SLP_S3_L

MCPCORES0_EN MAKE_BASE=TRUE

=MCPCORES0_EN OUT 74C6 Enable regulator DELAY OF ~16MS FROM PM_SLP_S3_L

C7080 0.47UF 10% 6.3V CERM-X5R 402

C7081 0.47UF 10% 6.3V CERM-X5R 402

C7082 0.47UF 10% 6.3V CERM-X5R 402

1.5V_S3 NEED TO BE ON BEFORE S0 FET ON

12V_S0 NEED TO BE ON BEFORE MCP REG AND 1.05_S0 REG EN

MXM POWER SEQUENCE

85B2 IN =PM_MXM_PGOOD_PULLUP

ALL_SYS_PWRGD_R MAKE_BASE=TRUE 70B1 6B7 7B4 7C3 7C4

PM_MXM_EN OUT 85B8

MXM CARD INPUT POWER ARE 12V_S0, 3V3_S0, 5V_S0
ALL_SYS_PWRGD ENABLES MXM REGULATORS

PM_MXM_PGOOD IS OPEN DRAIN SIGNAL, IT'S PULLED UP TO ALL_SYS_PWRGD

State	SMC_PM_G2_ENABLE (PORTABLES)	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

=PP3V3_S5_PWRCTL 6D1 70A3 70B1 70B3 70D8

R7031 1K 5% 1/16W MF-LF 402

79B4 PGOOD_1V05_S5

1V05V_S0 DERIVES FROM 3.3V_S5

RSMRST_PWRGD OUT 49D8 To SMC (2)

C7031 0.1UF 10% 16V X5R 402

FROM THIS SMC GENERATES PM_RSMRST_L WHICH GOES INTO PGOOD_S5 OF MCP
DELAY IS ABOUT 200MS

PGOOD Comparators

6C1 =PP12V_S5_PWRCTL

R7013 33.2K 1% 1/16W MF-LF 402

R7018 84.5K 1% 1/16W MF-LF 402

R7020 64.9K 1% 1/16W MF-LF 402

C7010 0.1UF 20% 16V CERM 603

XW7000 OMIT SM

7D3 6A6 53B4 51B3 PP12V_S0

R7000 4.99K 1% 1/16W MF-LF 402

12VS0_PG_CMP

XW7001 OMIT SM

6D3 =PPDDR_S3_PGCMP

R7001 1.21K 1% 1/16W MF-LF 402

1V5S3_PG_CMP

USING COMPARTOR INSTEAD OF REGULATOR
PGOOD_OUTPUT BECAUSE IF 5V_S5 DOES NOT COME UP, PDDDR_REGULATOR HAS NO INTERNAL POWER TO PULL PGOOD LOW

IG

R7002 2.0K 1% 1/16W MF-LF 402

6C4 =PP1V8_S0_PGCMP

XW7002 OMIT SM

1V8S0_PG_CMP

MXM

R7004 4.7K 1% 1/16W MF-LF 402

6A6 78D5 7D3 PP5V_S0

XW7003 OMIT SM

5VS0_PG_CMP

R7003 1.21K 1% 1/16W MF-LF 402

1V5S0_PG_CMP

XW7004 OMIT SM

54C5 7D3 6C6 54B6 PP1V5_S0

PLACE SHORTS CLOSE TO PLANE CUTS

CRITICAL

U7010 LM339A SOI-HF

V+ GND

(9.91V/9.58V; 330MV HYSTERESIS)

(1.30V/1.22V; 80MV HYSTERESIS)

1V60 IF 1.8V CMP
(1.67V/1.53V; 132MV HYSTERESIS)

4V12 IF 5V CMP
(4.51V/4.26V; 310MV HYSTERESIS)

(1.30V/1.22V; 80MV HYSTERESIS)

12VS5_9V00_REF	4	-1
12VS0_COMP_REF	5	+1
(12VS5_1V27_REF)	6	-2
1V5S3_COMP_REF	7	+2
12VS5_1V60_REF	8	-3
1V8S0_COMP_REF	9	+3
12VS5_1V27_REF	10	-4
1V5S0_COMP_REF	11	+4

OUT1 2 PGOOD_12V_S0 OUT 70C8

OUT2 1 PGOOD_1V5_S3 OUT 70C8

OUT3 14 PGOOD_1V8S0_OR_5VS0 OUT 70B4

OUT4 13 PGOOD_1V5_S0 OUT 70B4

(PULLUPS ARE NEAR LOADS)

R7005 49.9K 1% 1/16W MF-LF 402

R7006 49.9K 1% 1/16W MF-LF 402

R7007 49.9K 1% 1/16W MF-LF 402

R7008 49.9K 1% 1/16W MF-LF 402

R7014 100K 1% 1/16W MF-LF 402

R7019 10K 1% 1/16W MF-LF 402

R7021 10K 1% 1/16W MF-LF 402

HYSTERESIS NUMBERS CALCULATED BASED ON OUPTPUT PULL UP OF 3.3V

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S0341	1	RES,19.1K,1%,402	R7020		MXM

70D8 70C1 70B1 70A3 6D1 =PP3V3_S5_PWRCTL

R7033 10K 1% 1/16W MF-LF 402

70B4 PGOOD_1V8S0_OR_5VS0

70A4 PGOOD_1V5_S0

CAN I USE ALIAS OR DO I NEED INLINE RESISTOR?

S0 RAILS PGOOD

=PP3V3_S5_PWRCTL 6D1 70A3 70B3 70C1 70D8

C7020 0.1UF 20% 10V CERM 402

PLACE RESISTORS CLOSE TO U7020

6B4 =PP3V3_S0_PWRCTL

R7030 10K 5% 1/16W MF-LF 402

S0_PWR_CMP_PGOOD MAKE_BASE=TRUE

TC7SZ08AFEAPE SOT665

U7020

4 ALL_SYS_PWRGD

R7098 33 5% 1/16W MF-LF 402

ALL_SYS_PWRGD_SMC OUT 49D8

R7099 33 5% 1/16W MF-LF 402

ALL_SYS_PWRGD_R OUT 70D3 6B7 7B4 7C3 7C4

74C6 IN PGOOD_MCPCORE_S0

76B3 IN PGOOD_1V05_S0

S0_PWR_REG_PGOOD MAKE_BASE=TRUE

	I	Rds(on)	Vgs +/-
IRF7410	13A	7mOHM	8V
IRF7413	9.6A	18mOHM	20V
FDS4435	8.8A	35mOHM	25V
IRF7406	5.8A	70mOHM	20V
IRF6402	3.7A	65mOHM	12V
SI2302	1.6A	115mOHM	8V

70D8 70C1 70B3 70B1 6D1 =PP3V3_S5_PWRCTL

C7056 0.1uF 20% 10V CERM 402

85B3 85B8 IN PM_MXM_PGOOD

7C4 71C7 7C7 IN VR_PWRGOOD_DELAY

U7056 MC74VHC1G08 SOT23-5-HF

MCP_PS_PWRGD OUT 21B7

ALL_SYS_PWRGD IS ALSO AN INPUT TO THIS AND GATE BY THE FACT THAT PM_MXM_PGOOD IS PULLED UP TO IT

PGOOD and Power Sequencing

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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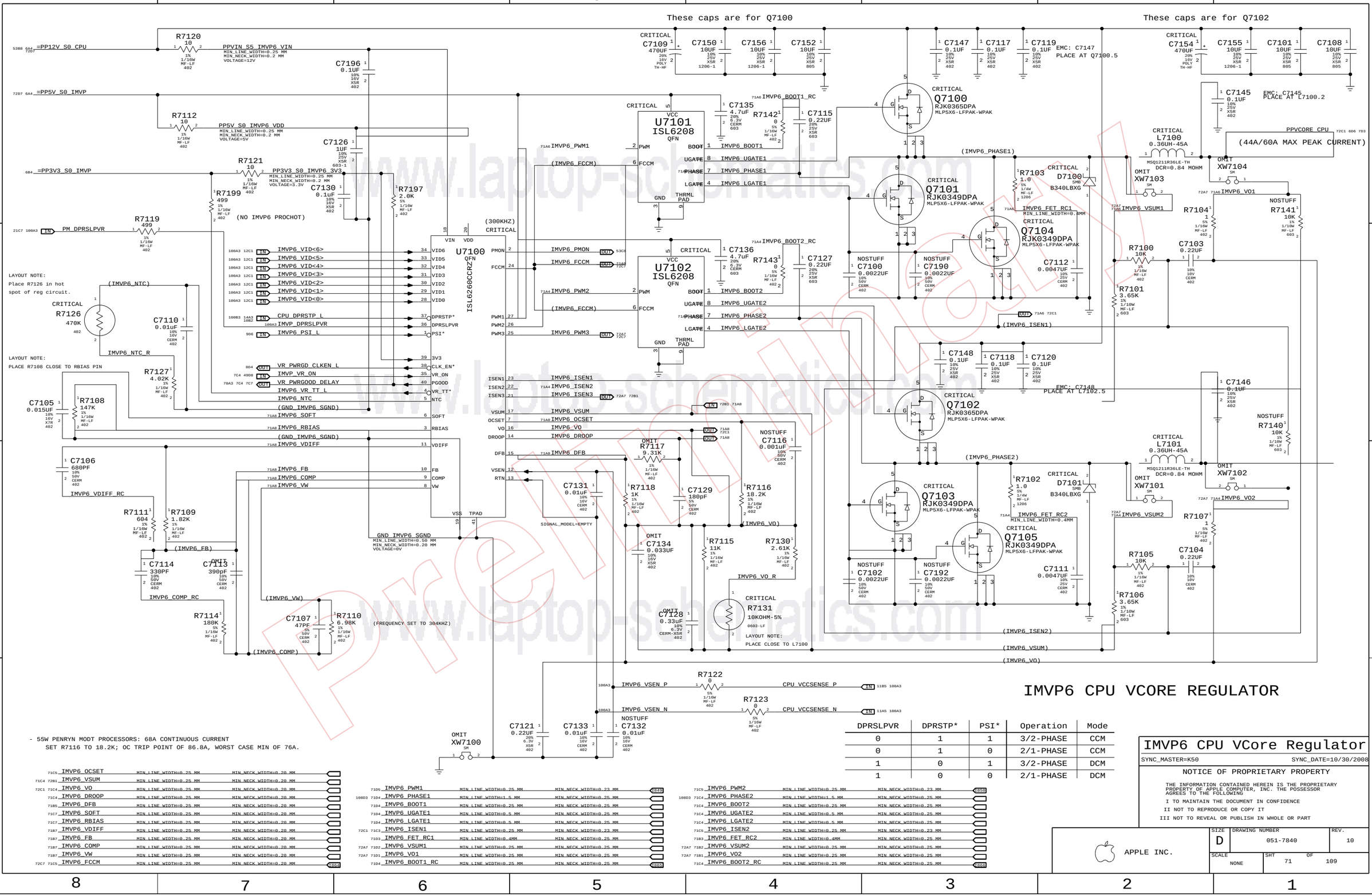

DPRSLPVR	DPRSTP*	PSI*	Operation	Mode
0	1	1	3/2-PHASE	CCM
0	1	0	2/1-PHASE	CCM
1	0	1	3/2-PHASE	DCM
1	0	0	2/1-PHASE	DCM

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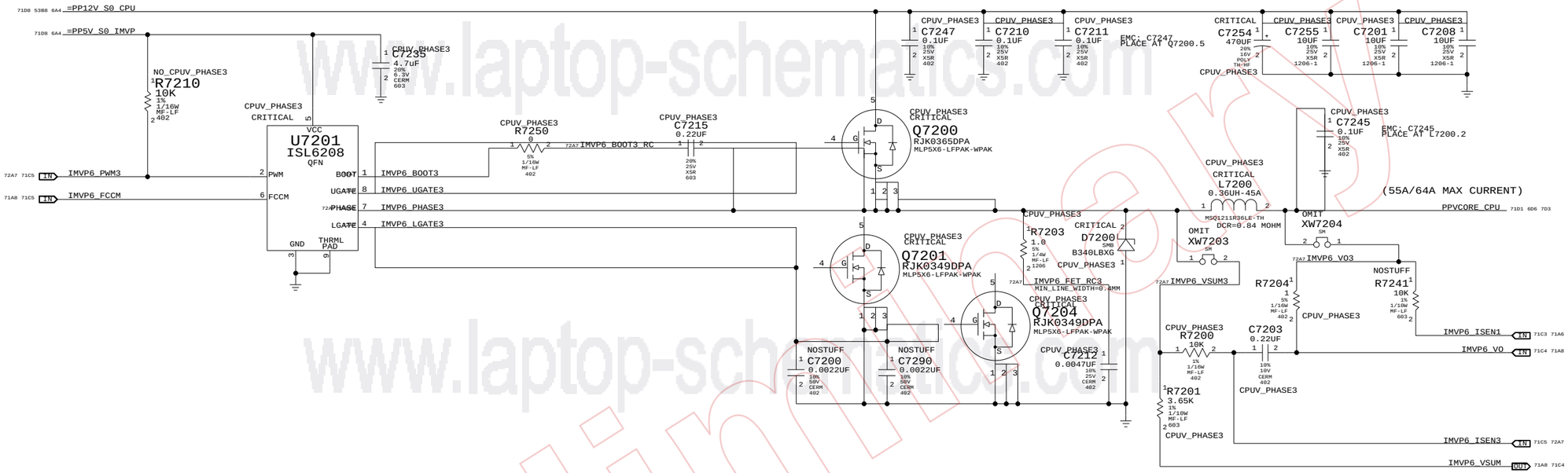
IMVP6 CPU VCORE REGULATOR



NO TEST FOR CPU VREG, ADDED K2/K3

IMVP6_VO1	NO_TEST=TRUE	
IMVP6_VO2	NO_TEST=TRUE	
IMVP6_VO3	NO_TEST=TRUE	
IMVP6_VSUM1	NO_TEST=TRUE	
IMVP6_VSUM2	NO_TEST=TRUE	
IMVP6_VSUM3	NO_TEST=TRUE	

IMVP6_PWM3	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.23 MM	T51
IMVP6_PHASE3	MIN_LINE_WIDTH=1.5 MM	MIN_NECK_WIDTH=0.25 MM	T43
IMVP6_BOOT3	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM	T44
IMVP6_UGATE3	MIN_LINE_WIDTH=0.5 MM	MIN_NECK_WIDTH=0.25 MM	T45
IMVP6_LGATE3	MIN_LINE_WIDTH=0.5 MM	MIN_NECK_WIDTH=0.25 MM	T46
IMVP6_ISEN3	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.23 MM	T48
IMVP6_FET_RC3	MIN_LINE_WIDTH=0.4MM	MIN_NECK_WIDTH=0.25 MM	T47
IMVP6_VSUM3	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM	T49
IMVP6_VO3	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM	T50
IMVP6_BOOT3_RC	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM	T52

IMVP6 3RD PHASE

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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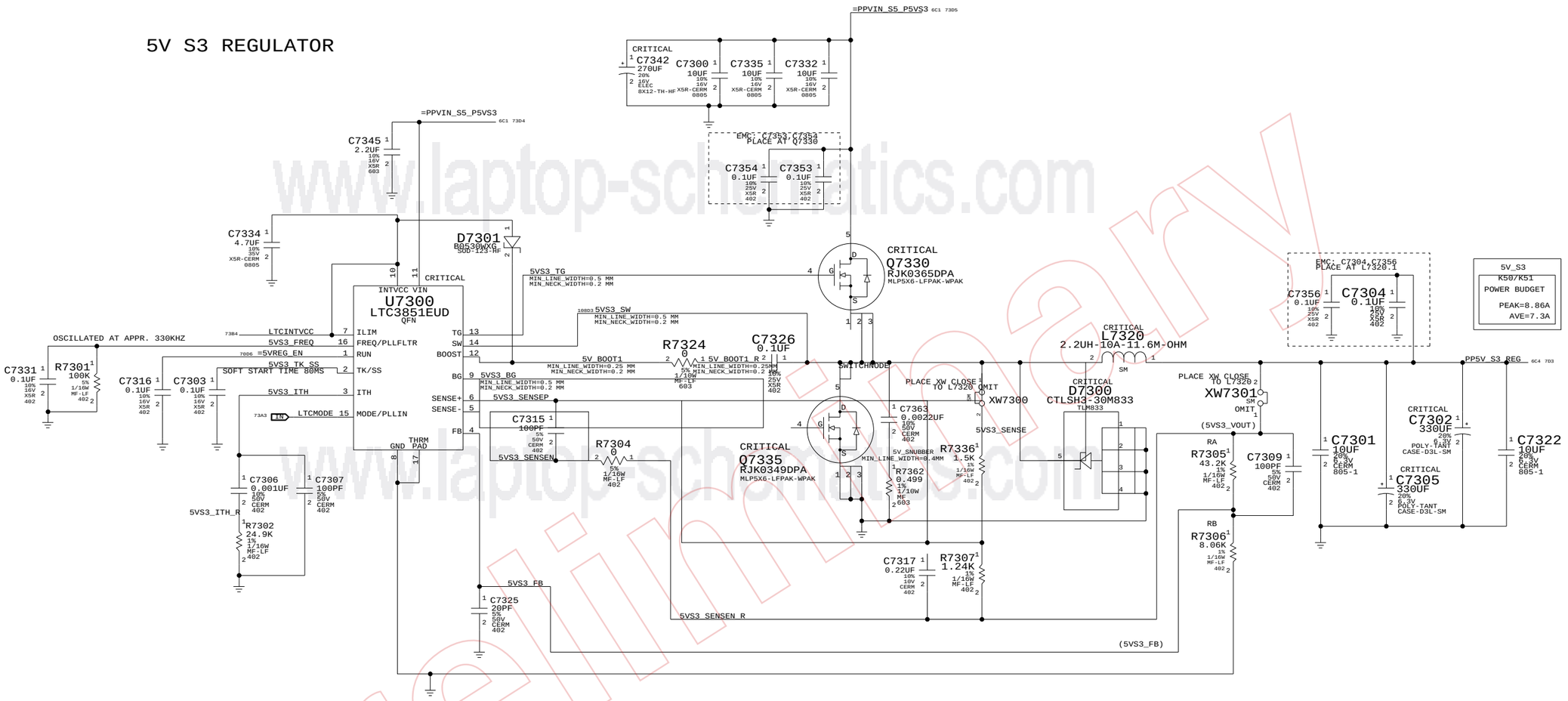
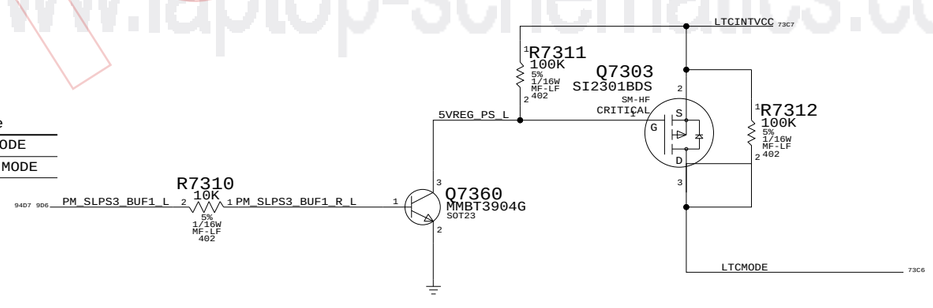
5V_S3 REGULATOR



STATE	PM_SLP3_BUF1_L	5VREG_PS_L	LTCMODE	Mode
S0	1	0	1	CONT MODE
S3	0	1	0	BURST MODE



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5V_S3 REGULATOR

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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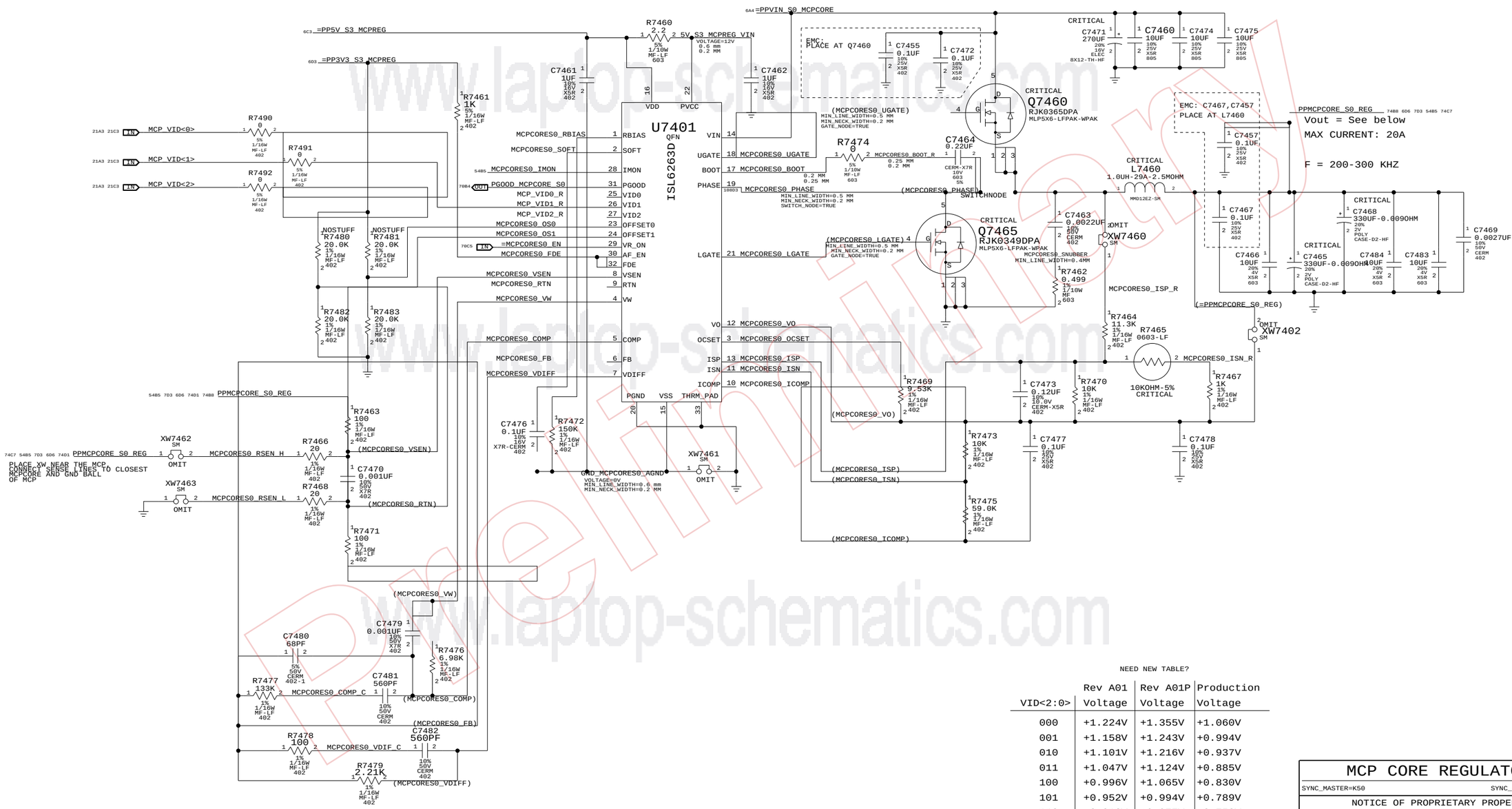
SCALE NONE SHT 73 OF 109

MCP CORE



NEED NEW TABLE?

VID<2:0>	Rev A01 Voltage	Rev A01P Voltage	Production Voltage
000	+1.224V	+1.355V	+1.060V
001	+1.158V	+1.243V	+0.994V
010	+1.101V	+1.216V	+0.937V
011	+1.047V	+1.124V	+0.885V
100	+0.996V	+1.065V	+0.830V
101	+0.952V	+0.994V	+0.789V
110	+0.913V	+0.977V	+0.752V
111	+0.876V	+0.917V	+0.719V

(Also A01Q)

MCP CORE REGULATOR

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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SIZE	DRAWING NUMBER	REV.
D	051-7840	10
SCALE: NONE	SHT 74 OF 109	

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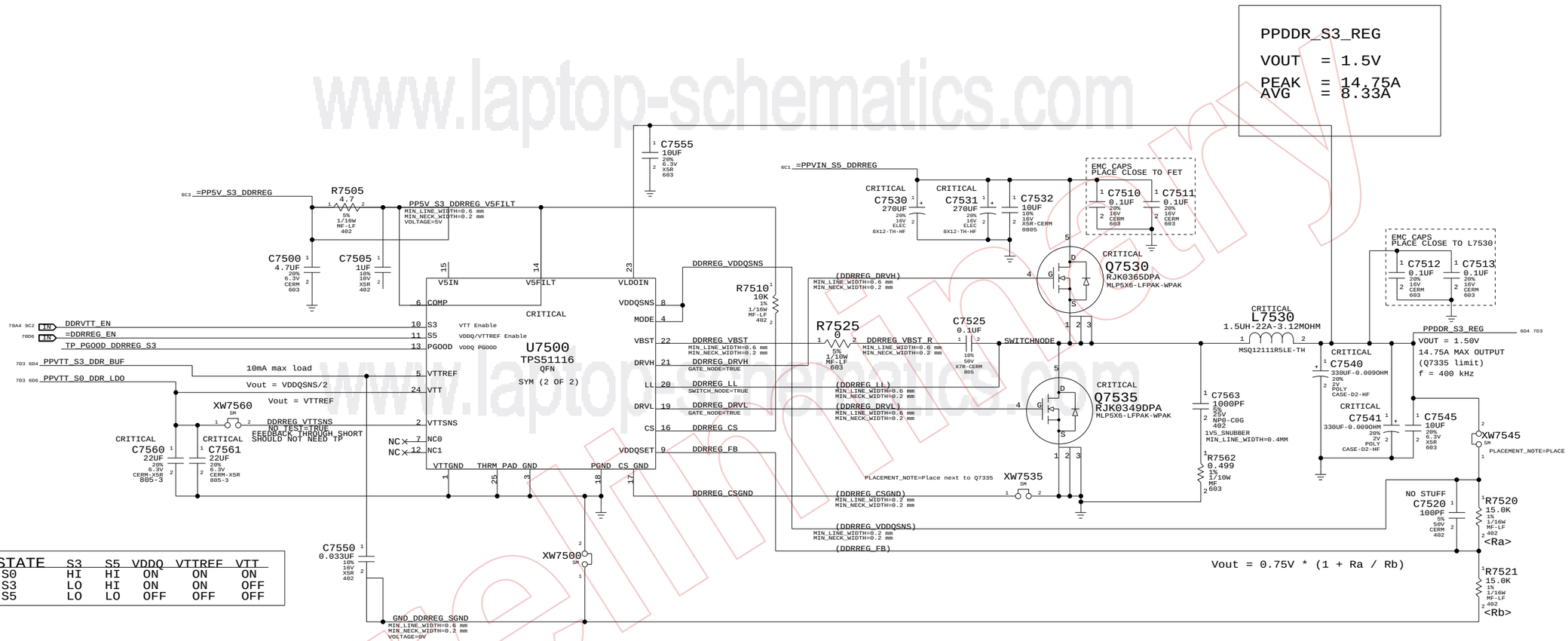
1.5 V DDR SUPPLY

PPDDR_S3_REG
VOUT = 1.5V
PEAK = 14.75A
AVG = 8.33A



STATE	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON
S3	LO	HI	ON	ON	OFF
S5	LO	LO	OFF	OFF	OFF

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1.5V DDR SUPPLY

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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SIZE	DRAWING NUMBER	REV.
D	051-7840	10

SCALE: NONE SHT 75 OF 109

3.3V S5 AND 1.05 S0 RAILS

INPUT POWER OF 12V_S0

6A4 =PPVIN_S0_P1V05S0

EMC CAPS PLACE CLOSE TO FET

C7613 10UF 10% 16V X5R-CERM 0805
C7612 10UF 10% 16V X5R-CERM 0805
C7610 10UF 10% 16V X5R-CERM 0805
C7611 0.1UF 20% 16V CERM 603
C7622 0.1UF 20% 16V CERM 603

CRITICAL
Q7610
FDMS9600S
MLP

(P1V05S0_UGATE)
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
GATE_NODE=TRUE

(P1V05S0_LGATE)
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
GATE_NODE=TRUE

SW

R7610 0 5% 1/10W MF-LF 603

P1V05S0_BOOT_R
MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.25MM

C7614 0.1UF 10% 50V X7R 603-1

MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.25MM

7D3 6D6 PP1V05_S0_REG

Vout = 1.058V
6.7A MAX OUTPUT
(R7614 LIMIT)
f = 200 kHz

CRITICAL
L7610
1.5UH-12A
MMD06EZ-SM

SWITCHNODE
PLACEMENT_NOTE=Place next to C7516

(P1V05S0_PHASE)
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
SWITCH_NODE=TRUE

C7615 10UF 10% 16V X5R-CERM 0805
C7617 10UF 10% 16V X5R-CERM 0805
CRITICAL
C7621 330UF-0.009OHM 20% 2V POLY CASE-D2-HF

C7623 0.1UF 20% 16V CERM 603
C7616 0.1UF 20% 16V CERM 603

EMC CAPS PLACE CLOSE TO L

1V05_S0
K507/K51
POWER BUDGET
PEAK=8.3A
AVE=4.4A

USING 0.5% RES SO RAIL NEVER LESS THAN 1.025V

C7662 1000PF 5% 25V NP0-C0G 402
XW7616 OMIT SM
1V05_SNUBBER MIN_LINE_WIDTH=0.4MM

R7663 0.499 1% 1/10W MF 603

P1V05S0_VSNS

R7620 5.23K 0.5% 1/16W MF 402 <Ra>

NO STUFF
C7620 100PF 5% 50V CERM 402

R7621 10.0K 0.5% 1/16W MF 402 <Rb>

Vout = 0.7V * (1 + Ra / Rb)

70C5 IN =1V05S0_EN

INPUT POWER OF 12V_S5

6C1 =PPVIN_S5_P3V3S5

EMC CAPS PLACE CLOSE TO FET

CRITICAL
C7681 100UF 20% 16V POLY 6.3X9-TH

C7680 10UF 10% 16V X5R-CERM 0805
C7683 10UF 10% 16V X5R-CERM 0805
C7624 0.1UF 20% 16V CERM 603
C7625 0.1UF 20% 16V CERM 603

6C1 =PP12V_S5_REG

R7650 2.2 5% 1/8W MF-LF 805

PPVIN_S5_3V3_1V05_R
VOLTAGE=12V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.20 MM

C7601 10UF 10% 16V X5R 1206

C7670 1UF 10% 16V X5R 603

PP5V_S5_LDO 6C2 7C3

C7689 4.7UF 20% 6.3V CERM 603

76A6 3V3REG_VCC
VOLTAGE=5V
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.1 MM

PVCC VCC

3V3S5_TG
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.20 MM

R7666 0 5% 1/16W MF-LF 603

3V3_BOOT2 0.25MM 0.2MM
23V3_BOOT2_R 0.25MM 0.2MM

C7666 0.1UF 10% 25V X5R 402

108D3 3V3S5_SW
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.20 MM
SWITCHNODE

CRITICAL
Q7660
FDMS9600S
MLP

SW

CRITICAL
L7660
2.2UH-10A-13.6MOHM
MMD06EZ-SM

(3.3V NOMINAL)

PP3V3_S5_REG 3B69 3B87 6B8 6D2 7C3

SEL A3V3 S5
K507/K51
POWER BUDGET
K50 PEAK=4.94A
K50 AVE=2.18A

C7663 1000PF 5% 25V NP0-C0G 402

R7662 0.499 1% 1/10W MF 603

XW7651 OMIT SM

C7691 0.1UF 20% 16V CERM 603
C7626 0.1UF 20% 16V CERM 603

EMC CAPS PLACE CLOSE TO L

C7694 10UF 20% 6.3V CERM 805-1

CRITICAL
C7693 330UF 20% 6.3V POLY-TANT CASE-D3L-SM

C7692 10UF 20% 6.3V CERM 805-1

ISL6237 QFN

6	VIN	LDO	7
17	BOOT1	LDOREFIN	8
15	UGATE1	BOOT2	24
16	PHASE1	UGATE2	26
18	LGATE1	PHASE2	25
10	OUT1	LGATE2	23
14	EN1	OUT2	30
9	BYP	EN2	27
11	FB1	REFIN2	32
12	ILIM1	ILIM2	31
29	SKIP*	REF	1
4	EN_LDO	POK1	13
2	TON	POK2	28
5	NC		
20	NC		
33	THRM_PAD	GND	21, 22

P1V05S0_BOOT
P1V05S0_UGATE
108D3 P1V05S0_PHASE
P1V05S0_LGATE
(=P1V05S0_EN)
P1V05S0_FB
P1V05S0_ILIM
EN LDO ASAP
76A6 3V3REG_TON

EN_REG_ASAP_AFTER_LDO_OUT
3V3S5_ILIM
3V3S5_REF
PGOOD_3V3_S5
3V3S5_OUT

3V3S5_BG
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.20 MM

3V3_SNUBBER
MIN_LINE_WIDTH=0.4MM

R7675 200K 5% 1/16W MF-LF 402

C7675 1UF 10% 16V X5R 603

PGOOD_1V05_S0 OUT 78B4

R7614 150K 1% 1/16W MF-LF 402

C7685 0.1UF 10% 16V X7R-CERM 402

R7667 121K 1% 1/16W MF-LF 402

GND_PP3VREG_SGND
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=0V

OMIT
XW7650 SM

SELECTS SWITCHING FREQUENCY

76C5 3V3REG_VCC

NOSTUFF
R7643 0 5% 1/16W MF-LF 402

76B5 3V3REG_TON

R7622 0 5% 1/16W MF-LF 402

76B4 3V3S5_REF

EN_LDO TIED TO 12V_S5 TO EN LDO FIRST & REGULATOR INTERNAL LOGIC GETS POWER
EN2 (3V3_S5) IS TIED TO VCC, TIED INTERNALLY TO PVCC
TIED EXTERNALLY TO LDO OUT. SO REGULATOR IS ENABLED
AS SOON AS LDO OUTPUT IS GOOD

EN1 (1.05_S0) CONTROLLED SEPARATELY

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Proprietary

1.05VS0/3.3V S5 SUPPLIES

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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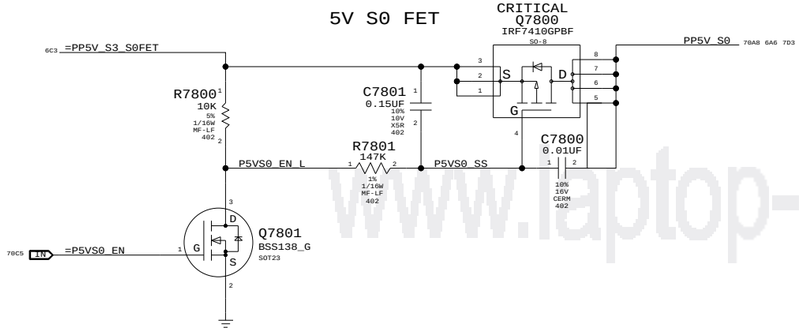
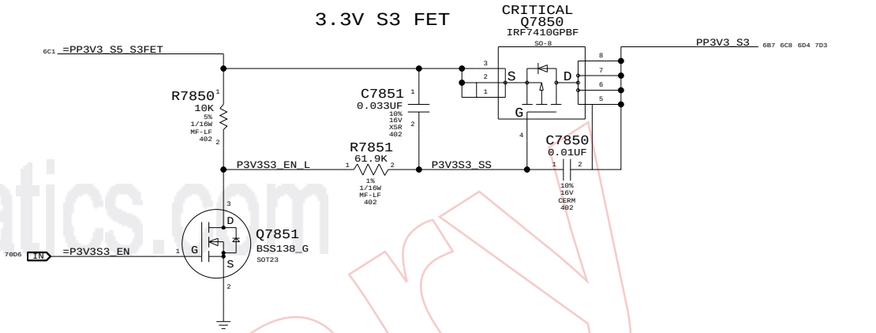
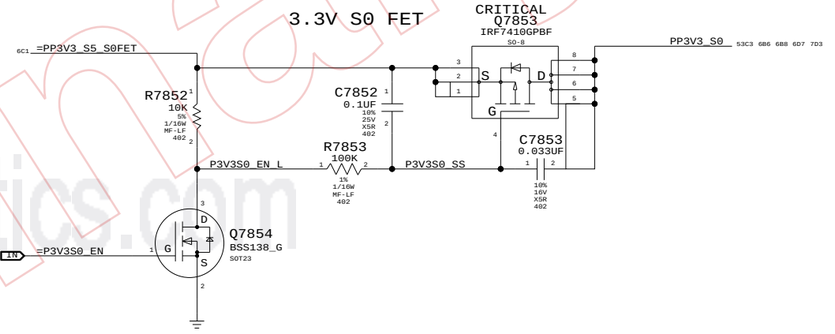
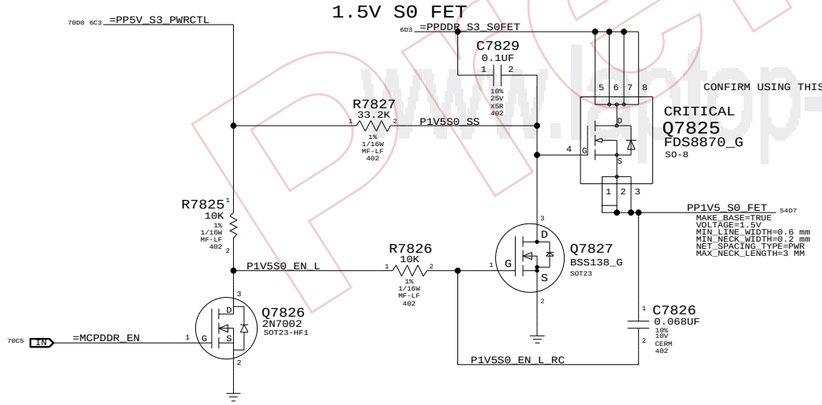
SIZE	DRAWING NUMBER	REV.
D	051-7840	10
SCALE: NONE	SHT 76 OF 109	



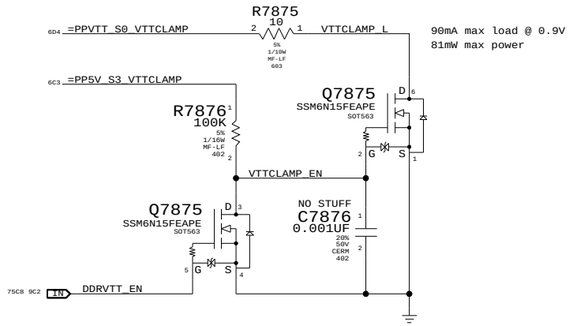






MCP79 DDRVTT FET

MCP79 DDR PAD LEAKAGE IS HIGH ENOUGH THAT
NVIDIA RECOMMENDS UNPOWERING DURING SLEEP.
IN ORDER TO SUPPORT UNPOWERING RAIL, HARDWARE
MUST GUARANTEE MEM_CKE SIGNALS ARE LOW
BEFORE RAIL IS TURNED OFF, AND REMAINS LOW
UNTIL AFTER RAIL TURNS BACK ON OR DIMMS
WILL EXIT SELF-REFRESH PREMATURELY.
MEM_VTT_EN OUTPUT FROM MCP79 USED TO ENABLE CLAMP
ON VTT RAIL, WHICH PULLS ALL CKE SIGNALS
LOW THROUGH VTT TERMINATION RESISTORS.



	I	Rds(on)	Vgs +/-
IRF7410	13A	7mOHM	8V
IRF7413	9.6A	18mOHM	20V
FDS4435	8.8A	35mOHM	25V
IRF7406	5.8A	70mOHM	20V
IRF6402	3.7A	65mOHM	12V
SI2302	1.6A	115mOHM	8V

S3 & S0 FETs

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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SCALE: NONE	SHT 78 OF 109	

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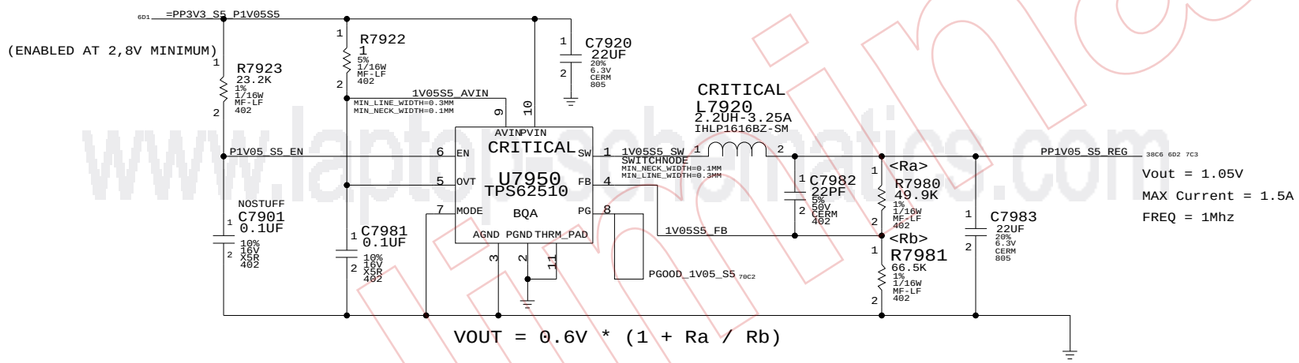
MCP 1.05V_S5 AUXC SUPPLY



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1V05 S5 POWER SUPPLY

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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SIZE	DRAWING NUMBER	REV.
D	051-7840	10

SCALE	SHT	OF
NONE	79	109

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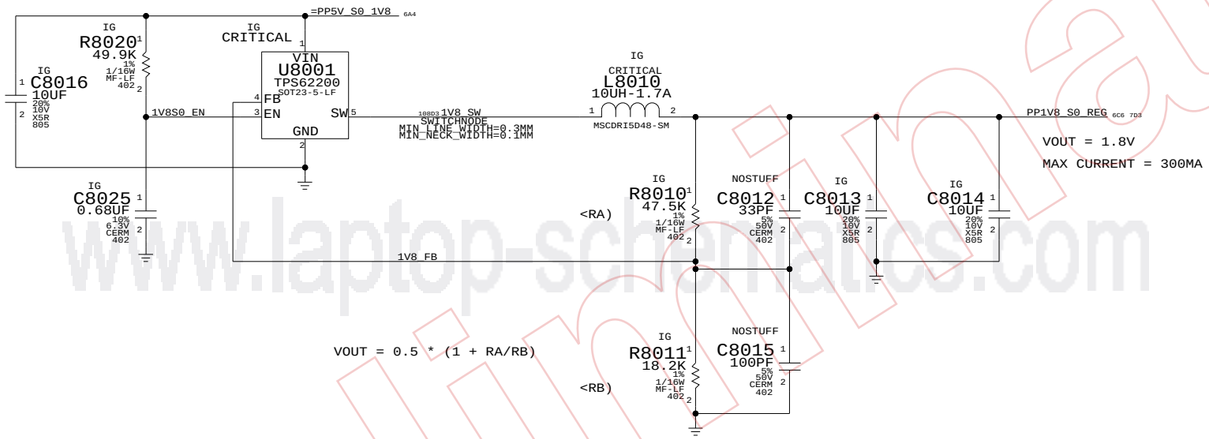
MCP ONLY 1.8V_S0 POWER SUPPLY



Preliminary
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1V8 POWER SUPPLY

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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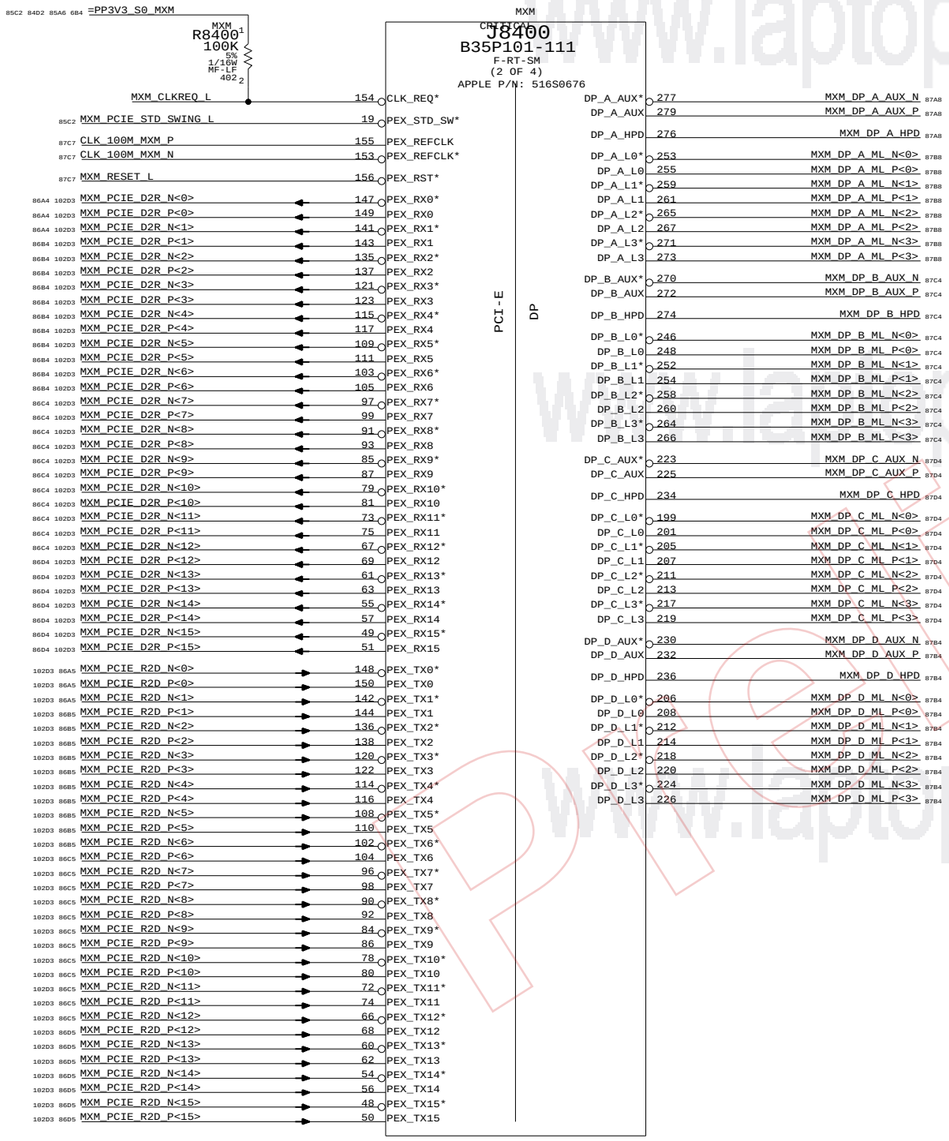
SIZE	DRAWING NUMBER	REV.
D	051-7840	10
SCALE: NONE	SHT 80 OF 109	

Page Notes

Power aliases required by this page:
- =PP3V3_S0_MXM
- =PP5V_S0_MXM
- =PPV_S0_MXM_PWRSRC

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- MXM



MXM SPEC POWER REQUIREMENTS
(NOT NECESSARILY THE SAME FOR EVERY MODULE)

VOLTAGE	CURRENT	POWER
3V3	1.0 A	3.3 W
5V	2.5 A	12.5 W
PWR (7-20V)	UP TO 10 A	PLATFORM DEPENDENT

MXM PCIe, DP & Power

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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SIZE	DRAWING NUMBER	REV.
D	051-7840	10

SCALE: NONE SHT 84 OF 109

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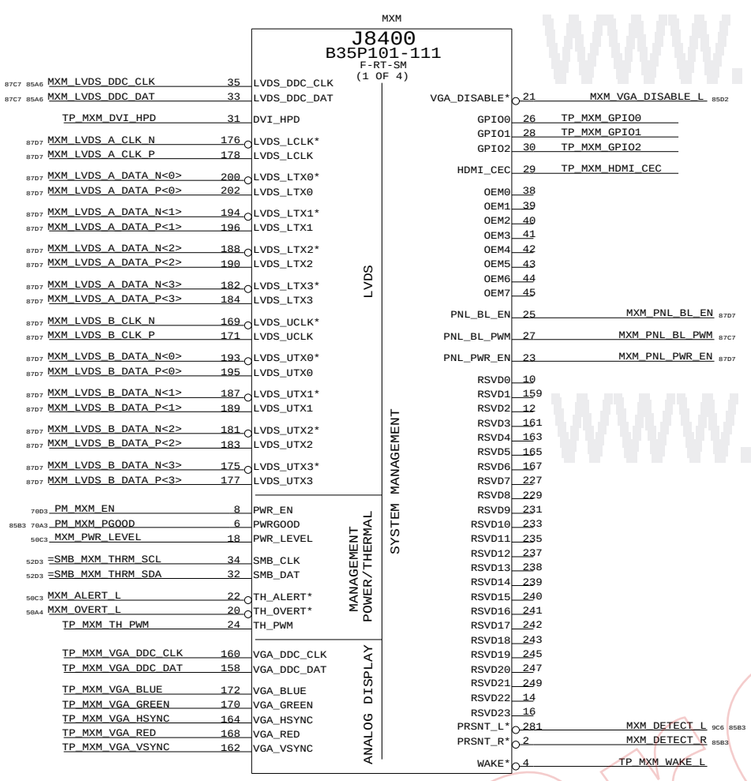
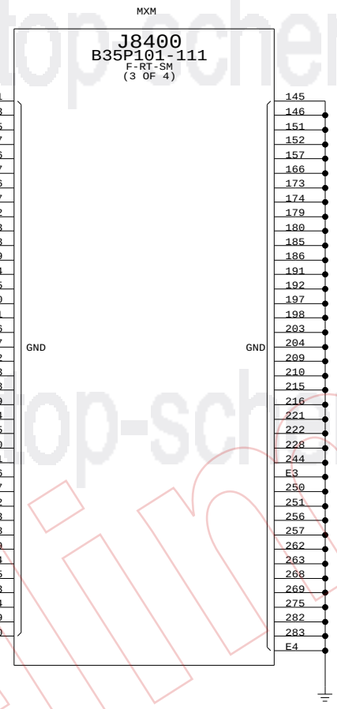
Page Notes

Power aliases required by this page:
- =PP3V3_S0_MXM

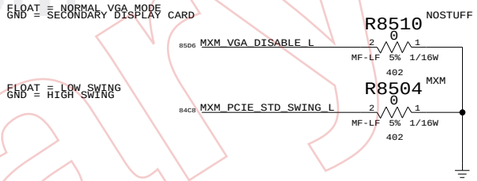
Signal aliases required by this page:
- =SMB_MXM_THRM_DATA
- =PM_MXM_PGOOD_PULLUP
- =SMB_MXM_THRM_CLK

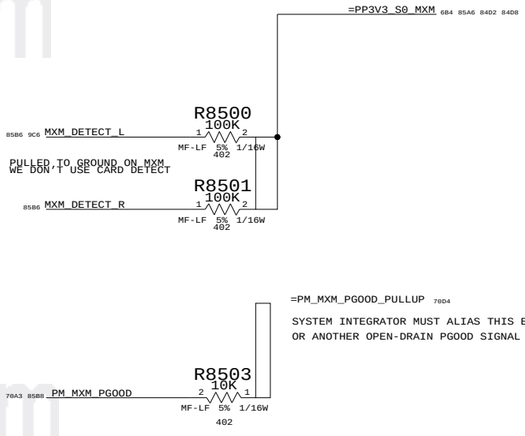
BOM options provided by this page:





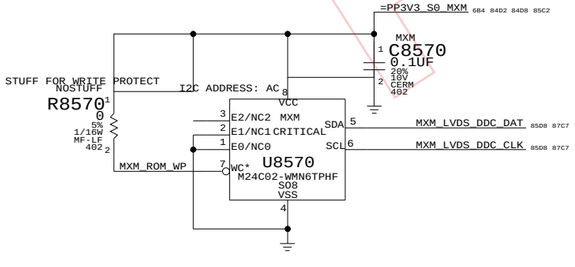
PULLUPS & PULLDOWNS AT MXM CONNECTOR





MXM SYSTEM INFORMATION ROM

PLACE CLOSE TO J7800



MXM I/O

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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SIZE	DRAWING NUMBER	REV.
D	051-7840	10
SCALE: NONE	SHT 85 OF 109	

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Preliminary

SLOTB MXM TX CAPS

102D3 9C6 IN	PEG_R2D_C_N<0>	MXM	C8600	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<15>	OUT 102D3 84A8
102D3 9C6 IN	PEG_R2D_C_P<0>	MXM	C8601	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_N<15>	OUT 102D3 84A8
102D3 9C6 IN	PEG_R2D_C_P<1>	MXM	C8602	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<14>	OUT 102D3 84A8
102D3 9C6 IN	PEG_R2D_C_N<1>	MXM	C8603	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_N<14>	OUT 102D3 84A8
102D3 9C6 IN	PEG_R2D_C_N<2>	MXM	C8604	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<13>	OUT 102D3 84A8
102D3 9C6 IN	PEG_R2D_C_P<2>	MXM	C8605	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_N<13>	OUT 102D3 84A8
102D3 9C6 IN	PEG_R2D_C_N<3>	MXM	C8606	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<12>	OUT 102D3 84A8
102D3 9C6 IN	PEG_R2D_C_P<3>	MXM	C8607	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_N<12>	OUT 102D3 84A8
102D3 9C6 IN	PEG_R2D_C_N<4>	MXM	C8608	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<11>	OUT 102D3 84A8
102D3 9C6 IN	PEG_R2D_C_P<4>	MXM	C8609	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_N<11>	OUT 102D3 84A8
102D3 9C6 IN	PEG_R2D_C_N<5>	MXM	C8610	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<10>	OUT 102D3 84A8
102D3 9C6 IN	PEG_R2D_C_P<5>	MXM	C8611	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_N<10>	OUT 102D3 84A8
102D3 9C6 IN	PEG_R2D_C_N<6>	MXM	C8612	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<9>	OUT 102D3 84A8
102D3 9C6 IN	PEG_R2D_C_P<6>	MXM	C8613	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_N<9>	OUT 102D3 84A8
102D3 9C6 IN	PEG_R2D_C_N<7>	MXM	C8614	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<8>	OUT 102D3 84A8
102D3 9C6 IN	PEG_R2D_C_P<7>	MXM	C8615	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_N<8>	OUT 102D3 84A8
102D3 9C6 IN	PEG_R2D_C_N<8>	MXM	C8616	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<7>	OUT 102D3 84A8
102D3 9C6 IN	PEG_R2D_C_P<8>	MXM	C8617	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_N<7>	OUT 102D3 84A8
102D3 9C6 IN	PEG_R2D_C_N<9>	MXM	C8618	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<6>	OUT 102D3 84B8
102D3 9C6 IN	PEG_R2D_C_P<9>	MXM	C8619	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_N<6>	OUT 102D3 84B8
102D3 9C6 IN	PEG_R2D_C_N<10>	MXM	C8620	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<5>	OUT 102D3 84B8
102D3 9C6 IN	PEG_R2D_C_P<10>	MXM	C8621	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_N<5>	OUT 102D3 84B8
102D3 9C6 IN	PEG_R2D_C_P<11>	MXM	C8622	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<4>	OUT 102D3 84B8
102D3 9C6 IN	PEG_R2D_C_N<11>	MXM	C8623	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_N<4>	OUT 102D3 84B8
102D3 9C6 IN	PEG_R2D_C_N<12>	MXM	C8624	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<3>	OUT 102D3 84B8
102D3 9C6 IN	PEG_R2D_C_P<12>	MXM	C8625	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_N<3>	OUT 102D3 84B8
102D3 9C6 IN	PEG_R2D_C_N<13>	MXM	C8626	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<2>	OUT 102D3 84B8
102D3 9C6 IN	PEG_R2D_C_P<13>	MXM	C8627	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_N<2>	OUT 102D3 84B8
102D3 9C6 IN	PEG_R2D_C_N<14>	MXM	C8628	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<1>	OUT 102D3 84B8
102D3 9C6 IN	PEG_R2D_C_P<14>	MXM	C8629	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_N<1>	OUT 102D3 84B8
102D3 9C6 IN	PEG_R2D_C_N<15>	MXM	C8630	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<0>	OUT 102D3 84B8
102D3 9C6 IN	PEG_R2D_C_P<15>	MXM	C8631	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_N<0>	OUT 102D3 84B8

SLOTB MXM RX CAPS

102D3 84B8 IN	MXM_PCIE_D2R_P<15>	MXM	C8632	0.1UF	2 10% 16V X5R 402	PEG_D2R_N<0>	OUT 102D3 9C6
102D3 84B8 IN	MXM_PCIE_D2R_N<15>	MXM	C8633	0.1UF	2 10% 16V X5R 402	PEG_D2R_P<0>	OUT 102D3 9C6
102D3 84B8 IN	MXM_PCIE_D2R_P<14>	MXM	C8634	0.1UF	2 10% 16V X5R 402	PEG_D2R_P<1>	OUT 102D3 9C6
102D3 84B8 IN	MXM_PCIE_D2R_N<14>	MXM	C8635	0.1UF	2 10% 16V X5R 402	PEG_D2R_N<1>	OUT 102D3 9C6
102D3 84B8 IN	MXM_PCIE_D2R_P<13>	MXM	C8636	0.1UF	2 10% 16V X5R 402	PEG_D2R_P<2>	OUT 102D3 9C6
102D3 84B8 IN	MXM_PCIE_D2R_N<13>	MXM	C8637	0.1UF	2 10% 16V X5R 402	PEG_D2R_N<2>	OUT 102D3 9C6
102D3 84B8 IN	MXM_PCIE_D2R_P<12>	MXM	C8638	0.1UF	2 10% 16V X5R 402	PEG_D2R_P<3>	OUT 102D3 9C6
102D3 84B8 IN	MXM_PCIE_D2R_N<12>	MXM	C8639	0.1UF	2 10% 16V X5R 402	PEG_D2R_N<3>	OUT 102D3 9C6
102D3 84B8 IN	MXM_PCIE_D2R_P<11>	MXM	C8640	0.1UF	2 10% 16V X5R 402	PEG_D2R_N<4>	OUT 102D3 9C6
102D3 84B8 IN	MXM_PCIE_D2R_N<11>	MXM	C8641	0.1UF	2 10% 16V X5R 402	PEG_D2R_P<4>	OUT 102D3 9C6
102D3 84B8 IN	MXM_PCIE_D2R_P<10>	MXM	C8642	0.1UF	2 10% 16V X5R 402	PEG_D2R_N<5>	OUT 102D3 9C6
102D3 84B8 IN	MXM_PCIE_D2R_N<10>	MXM	C8643	0.1UF	2 10% 16V X5R 402	PEG_D2R_P<5>	OUT 102D3 9C6
102D3 84C8 IN	MXM_PCIE_D2R_P<9>	MXM	C8644	0.1UF	2 10% 16V X5R 402	PEG_D2R_P<6>	OUT 102D3 9C6
102D3 84C8 IN	MXM_PCIE_D2R_N<9>	MXM	C8645	0.1UF	2 10% 16V X5R 402	PEG_D2R_N<6>	OUT 102D3 9C6
102D3 84C8 IN	MXM_PCIE_D2R_P<8>	MXM	C8646	0.1UF	2 10% 16V X5R 402	PEG_D2R_N<7>	OUT 787 102D3 9C6
102D3 84C8 IN	MXM_PCIE_D2R_N<8>	MXM	C8647	0.1UF	2 10% 16V X5R 402	PEG_D2R_P<7>	OUT 787 102D3 9C6
102D3 84C8 IN	MXM_PCIE_D2R_P<7>	MXM	C8648	0.1UF	2 10% 16V X5R 402	PEG_D2R_N<8>	OUT 102D3 9C6
102D3 84C8 IN	MXM_PCIE_D2R_N<7>	MXM	C8649	0.1UF	2 10% 16V X5R 402	PEG_D2R_P<8>	OUT 102D3 9C6
102D3 84C8 IN	MXM_PCIE_D2R_P<6>	MXM	C8650	0.1UF	2 10% 16V X5R 402	PEG_D2R_N<9>	OUT 102D3 9C6
102D3 84C8 IN	MXM_PCIE_D2R_N<6>	MXM	C8651	0.1UF	2 10% 16V X5R 402	PEG_D2R_P<9>	OUT 102D3 9C6
102D3 84C8 IN	MXM_PCIE_D2R_P<5>	MXM	C8652	0.1UF	2 10% 16V X5R 402	PEG_D2R_N<10>	OUT 102D3 9C6
102D3 84C8 IN	MXM_PCIE_D2R_N<5>	MXM	C8653	0.1UF	2 10% 16V X5R 402	PEG_D2R_P<10>	OUT 102D3 9C6
102D3 84C8 IN	MXM_PCIE_D2R_P<4>	MXM	C8654	0.1UF	2 10% 16V X5R 402	PEG_D2R_N<11>	OUT 102D3 9C6
102D3 84C8 IN	MXM_PCIE_D2R_N<4>	MXM	C8655	0.1UF	2 10% 16V X5R 402	PEG_D2R_P<11>	OUT 102D3 9C6
102D3 84C8 IN	MXM_PCIE_D2R_P<3>	MXM	C8656	0.1UF	2 10% 16V X5R 402	PEG_D2R_N<12>	OUT 102D3 9C6
102D3 84C8 IN	MXM_PCIE_D2R_N<3>	MXM	C8657	0.1UF	2 10% 16V X5R 402	PEG_D2R_P<12>	OUT 102D3 9C6
102D3 84C8 IN	MXM_PCIE_D2R_P<2>	MXM	C8658	0.1UF	2 10% 16V X5R 402	PEG_D2R_N<13>	OUT 102D3 9C6
102D3 84C8 IN	MXM_PCIE_D2R_N<2>	MXM	C8659	0.1UF	2 10% 16V X5R 402	PEG_D2R_P<13>	OUT 102D3 9C6
102D3 84C8 IN	MXM_PCIE_D2R_P<1>	MXM	C8662	0.1UF	2 10% 16V X5R 402	PEG_D2R_P<14>	OUT 102D3 9C6
102D3 84C8 IN	MXM_PCIE_D2R_N<1>	MXM	C8663	0.1UF	2 10% 16V X5R 402	PEG_D2R_N<14>	OUT 102D3 9C6
102D3 84C8 IN	MXM_PCIE_D2R_P<0>	MXM	C8660	0.1UF	2 10% 16V X5R 402	PEG_D2R_N<15>	OUT 102D3 9C6
102D3 84C8 IN	MXM_PCIE_D2R_N<0>	MXM	C8661	0.1UF	2 10% 16V X5R 402	PEG_D2R_P<15>	OUT 102D3 9C6

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MXM PCIE CAPS

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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D	051-7840	10
SCALE: NONE	SHT 86 OF 109	

Page Notes

Power aliases required by this page:
- =PP5V_DP_AUX

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

MXM

85C8 MXM_LVDS_A_DATA_P<3..0> = LVDS_EG_A_DATA_P<3..0> 107C2 89B6 89C6 89D6 90A6 90A8
85C8 MXM_LVDS_A_DATA_N<3..0> = LVDS_EG_A_DATA_N<3..0> 107C2 89B6 89C6 89D6 90A6 90A8
85C8 MXM_LVDS_B_DATA_P<3..0> = LVDS_EG_B_DATA_P<3..0> 107C2 89A6 89C3 89D3 90A8 90B6
85C8 MXM_LVDS_B_DATA_N<3..0> = LVDS_EG_B_DATA_N<3..0> 107C2 89A6 89C3 89D3 90A6 90B8

85C8 MXM_LVDS_A_CLK_N = LVDS_EG_A_CLK_N 89B6 107C2
85C8 MXM_LVDS_A_CLK_P = LVDS_EG_A_CLK_P 89B6 107C2
85C8 MXM_LVDS_B_CLK_N = LVDS_EG_B_CLK_N 89C3 107C2
85C8 MXM_LVDS_B_CLK_P = LVDS_EG_B_CLK_P 89C3 107C2

85C6 MXM_PNL_BL_EN = LVDS_BKL_ON 6D6 8D3 90A3 90C4
85C6 MXM_PNL_PWR_EN = LVDS_EG_PANEL_PWR 90A3 90B8
85C6 MXM_PNL_BL_PWM = LVDS_EG_BKL_PWM 90D6
85D8 85A6 MXM_LVDS_DDC_DAT = LVDS_EG_DDC_DATA 89A3 90A6
85D8 85A6 MXM_LVDS_DDC_CLK = LVDS_EG_DDC_CLK 89B3 90A8

84C8 CLK_100M_MXM_P = GPU_CLK100M_PCIE_P 9C6 102C3
84C8 CLK_100M_MXM_N = GPU_CLK100M_PCIE_N 9C6 102C3 7C3

84C8 MXM_RESET_L = PEG_RESET_L 9C2 90D4

EXTERNAL DP CONN

THESE ALIASES ARE TO CONFORM WITH K50/K52 SHARED CONNECTOR PAGE

84C5 MXM_DP_A_ML_N<0> = DP_EG_ML_N<0> 107D2 91D8
84C5 MXM_DP_A_ML_P<0> = DP_EG_ML_P<0> 107D2 91C8
84C5 MXM_DP_A_ML_N<1> = DP_EG_ML_N<1> 107D2 91C8
84C5 MXM_DP_A_ML_P<1> = DP_EG_ML_P<1> 107D2 91C8
84C5 MXM_DP_A_ML_N<2> = DP_EG_ML_N<2> 107D2 91B8
84C5 MXM_DP_A_ML_P<2> = DP_EG_ML_P<2> 107D2 91B7
84C5 MXM_DP_A_ML_N<3> = DP_EG_ML_N<3> 107D2 91C4
84C5 MXM_DP_A_ML_P<3> = DP_EG_ML_P<3> 107D2 91C4

84C5 MXM_DP_A_HPD = DP_EG_HPD 91B4

84D6 MXM_DP_A_AUX_N = DP_EG_AUXCH_N 93C4 107D2
84C6 MXM_DP_A_AUX_P = DP_EG_AUXCH_P 93B4 107D2

UNUSED DP INTERFACES

84B6 MXM_DP_C_ML_N<0..3> = TP_MXM_DP_C_ML_N<0..3>
84B6 MXM_DP_C_ML_P<0..3> = TP_MXM_DP_C_ML_P<0..3>
84C5 MXM_DP_C_AUX_N = TP_MXM_DP_C_AUX_N
84C5 MXM_DP_C_AUX_P = TP_MXM_DP_C_AUX_P
84B6 MXM_DP_C_HPD = TP_MXM_DP_C_HPD

84C5 MXM_DP_B_ML_N<0..3> = TP_MXM_DP_B_ML_N<0..3>
84C5 MXM_DP_B_ML_P<0..3> = TP_MXM_DP_B_ML_P<0..3>
84C5 MXM_DP_B_AUX_N = TP_MXM_DP_B_AUX_N
84C5 MXM_DP_B_AUX_P = TP_MXM_DP_B_AUX_P
84C5 MXM_DP_B_HPD = TP_MXM_DP_B_HPD

84B5 MXM_DP_D_ML_N<0..3> = TP_MXM_DP_D_ML_N<0..3>
84B5 MXM_DP_D_ML_P<0..3> = TP_MXM_DP_D_ML_P<0..3>
84B5 MXM_DP_D_AUX_N = TP_MXM_DP_D_AUX_N
84B5 MXM_DP_D_AUX_P = TP_MXM_DP_D_AUX_P
84B5 MXM_DP_D_HPD = TP_MXM_DP_D_HPD

All aliases: MAKE_BASE=TRUE

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MXM ALIASES

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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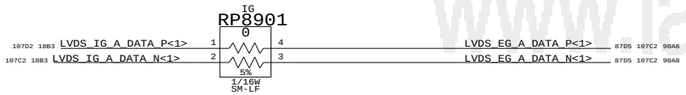

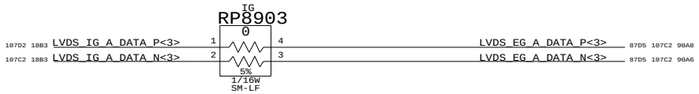

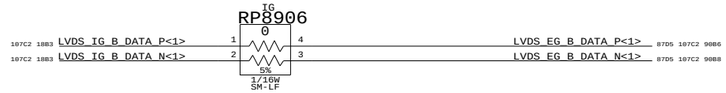

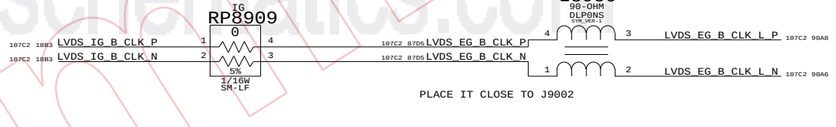

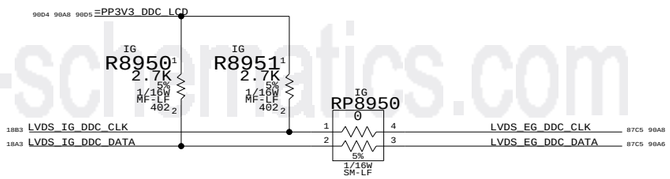

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LVDS MUX RESISTORS

SYNC_MASTER=SIJI SYNC_DATE=10/15/2008

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SIZE	DRAWING NUMBER	REV.
D	051-7840	10
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Page Notes

Power aliases required by this page:

- =PPV_S0_LCD_20INCH
- =PP3V3_S0_VIDEO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
IG, MXM

INVERTER INTERFACE

=PP3V3_S0_VIDEO

=PP3V3_DDC_LCD

LVDS_IG_BKL_PWM

IG R9075 0 5% 1/16W MF-LF 402

MXM R9080 0 5% 1/16W MF-LF 402

IG R9074 1K 5% 1/16W MF-LF 402

MXM R9079 0 5% 1/16W MF-LF 402

LVDS_EG_BKL_PWM

NOSTUFF R9078 10K 5% 1/16W MF-LF 402

LCD_PWM_MUX

=PP3V3_DDC_LCD

IG C9051 0.1UF 20% 10V CERM 402

IG C9050 0.1UF 20% 10V CERM 402

IG U9020 TC7SZ08AFEAPE 507965

PEG_RESET_L

LCD_PWM_GATE1

IG U9021 TC7SZ08AFEAPE 507665

LVDS_BKL_ON

LCD_PWM_R

R9081 47 5% 1/16W MF-LF 402

LCD_PWM_FILT

CRITICAL L9050 FERR-250-OHM SM

LCD_PWM

INVERTER CONNECTOR INCORPORATED INTO AC/DC CONNECTOR

LCD (LVDS) INTERFACE

PANEL POWER SEQUENCING

=PPV_S0_LCD_24INCH

VOLTAGE=5V MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm

R9000 100K 5% 1/16W MF-LF 402

C9000 0.1UF 10% 50V X7R 603-1

LCD_PWREN_DIV

R9001 29.4K 1% 1/16W MF-LF 402

R9002 100K 5% 1/16W MF-LF 402

CRITICAL Q9000 FDC638P_G SM

PPV_LCD_SW

VOLTAGE=12V MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm

L9000 FERR-250-OHM SM

VOLTAGE=12V MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm

PPV_LCD_CONN

12V FOR 24 INCH LCD

C9020 10UF 10% 16V X5R-CERM 1210

C9001 0.001uF 20% 50V CERM 402

LCD_PWREN_L_RC

PLACE NEAR J9002

LCD_PWREN_DIV_L

Q9001 2N7002 SOT23-HF1

LVDS_EG_PANEL_PWR

R9070 100K 5% 1/16W MF-LF 402

CRITICAL SDF9000 STDOFF-4.0OD4.6H-1.35-2.4-TH

516S0241

CRITICAL J9002 53307-8630 F-ST-SM

LVDS_EG_B_DATA_N<0>	1	2	LVDS_EG_B_DATA_P<0>
LVDS_EG_B_DATA_N<1>	3	4	LVDS_EG_B_DATA_P<1>
LVDS_EG_B_DATA_N<2>	5	6	LVDS_EG_B_DATA_P<2>
	7	8	LVDS_EG_B_CLK_L_N
LVDS_EG_B_CLK_L_P	9	10	LVDS_EG_B_DATA_N<3>
LVDS_EG_B_DATA_P<3>	11	12	LVDS_EG_A_DATA_N<0>
LVDS_EG_A_DATA_P<0>	13	14	
LVDS_EG_A_DATA_N<1>	15	16	LVDS_EG_A_DATA_P<1>
LVDS_EG_A_DATA_P<2>	17	18	LVDS_EG_A_DATA_N<2>
LVDS_EG_A_CLK_L_P	19	20	LVDS_EG_A_CLK_L_N
LVDS_EG_A_DATA_P<3>	21	22	LVDS_EG_A_DATA_N<3>
=PP3V3_DDC_LCD	23	24	
LVDS_EG_DDC_CLK	25	26	LVDS_EG_DDC_DATA
PPV_LCD_CONN	27	28	PPV_LCD_CONN
	29	30	

Panel has 4.7K DDC pull-ups
MXM also has 2.2K pull-ups

C9010 0.001uF 20% 50V CERM 402

CRITICAL SDF9001 STDOFF-4.0OD4.6H-1.35-2.4-TH

IG R9050 0 5% 1/16W MF-LF 402

LVDS_IG_BKL_ON

LVDS_BKL_ON

IG R9051 0 5% 1/16W MF-LF 402

LVDS_IG_PANEL_PWR

LVDS_EG_PANEL_PWR

IG R9060 1K 5% 1/16W MF-LF 402

IG R9061 1K 5% 1/16W MF-LF 402

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INTERNAL DISPLAY CONNS

SYNC_MASTER=SIJI SYNC_DATE=10/15/2008

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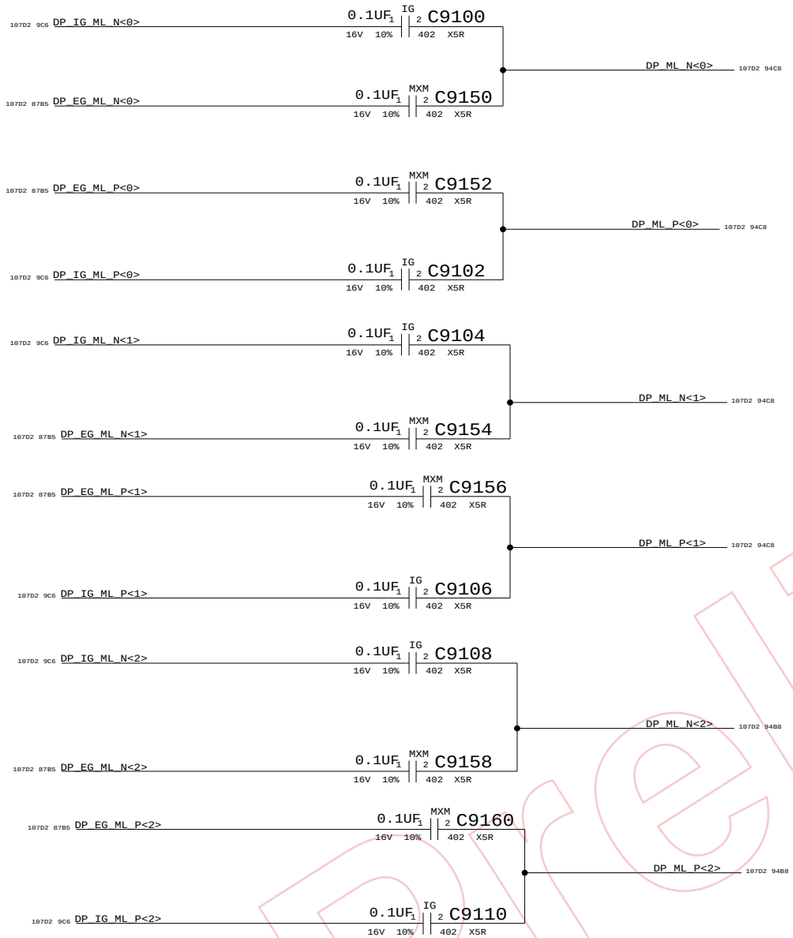

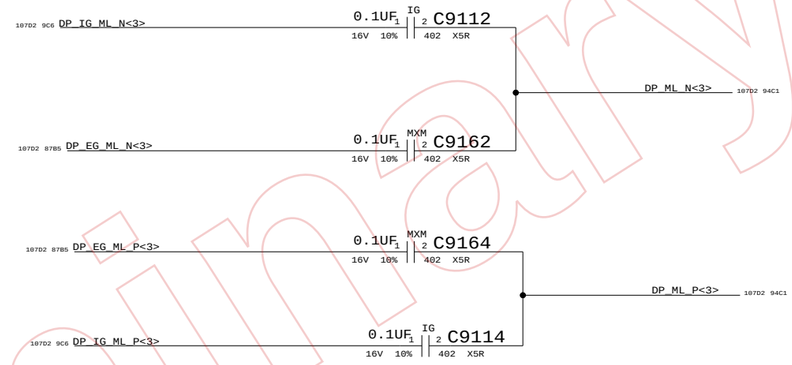

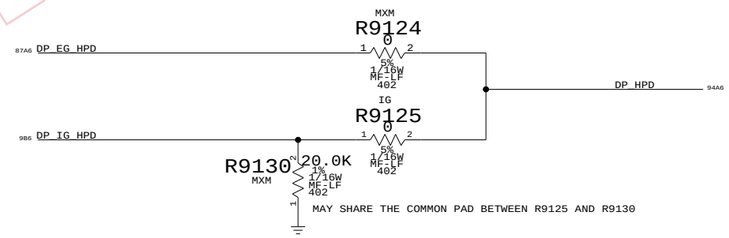

PLACE THESE CAPACITORS ATLEAST 1INCH AWAY FROM DP CONNECTOR

DP MUX SUPPORT

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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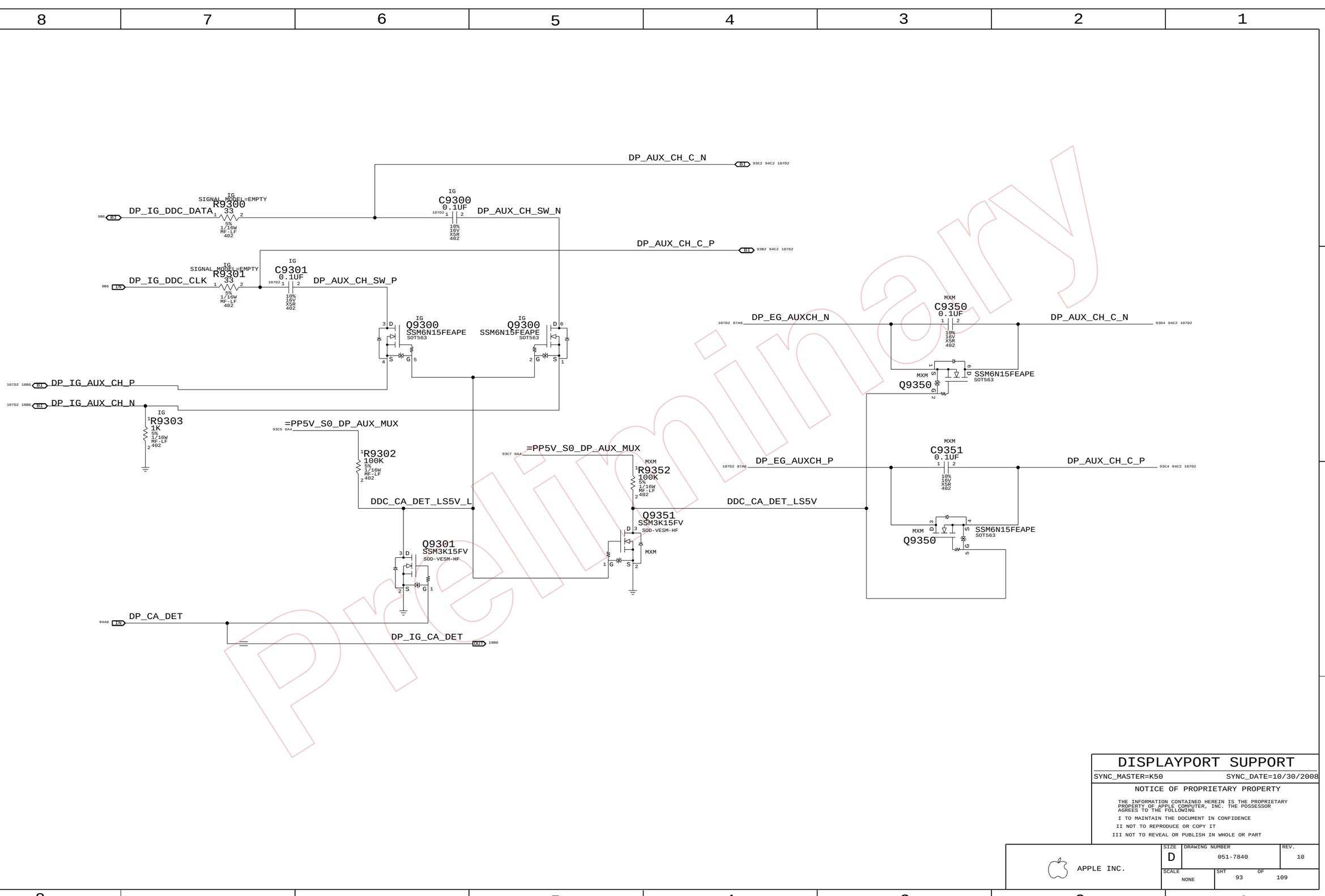

DISPLAYPORT SUPPORT

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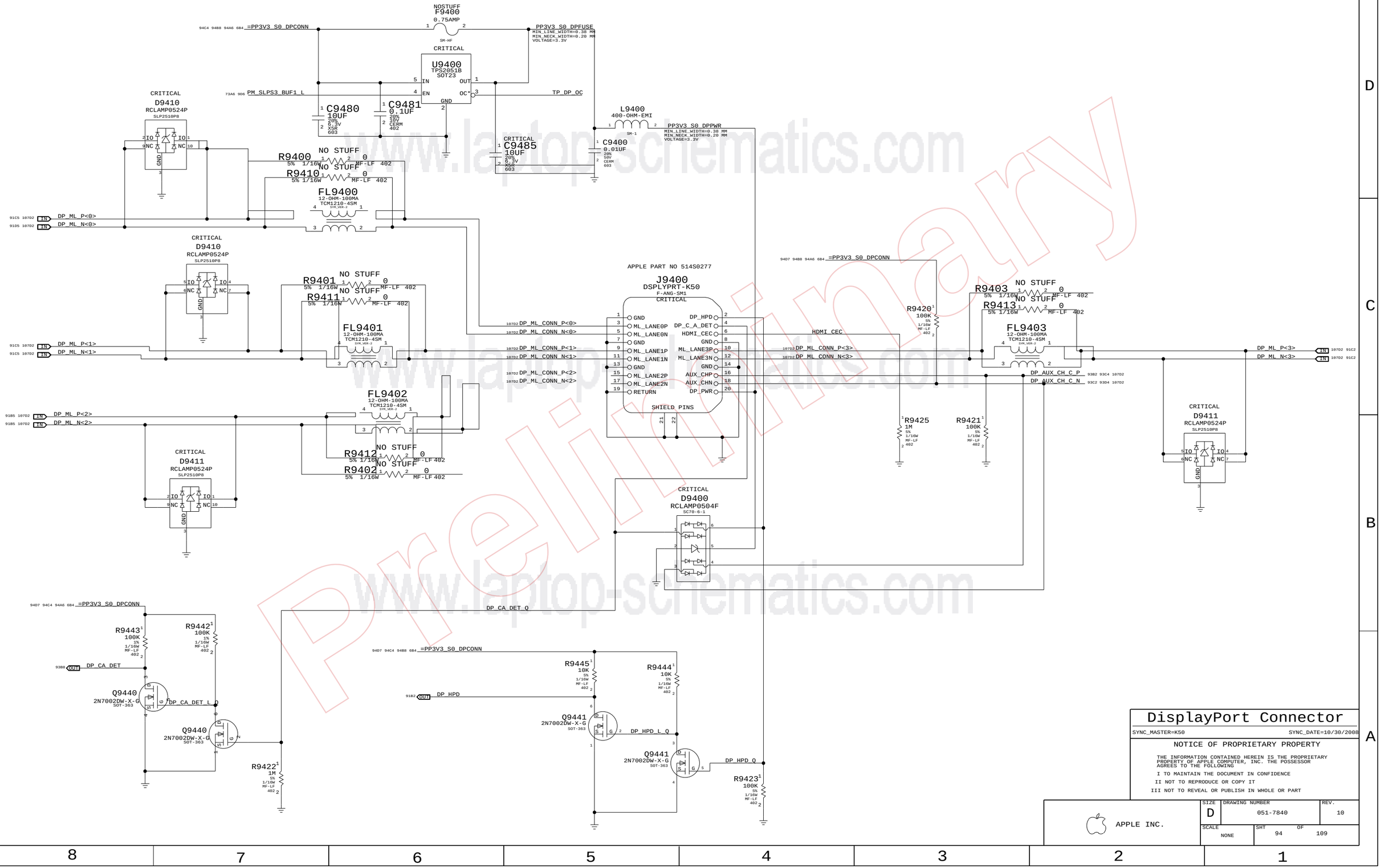
D	051-7840	10

SCALE	SHT	OF
NONE	93	109



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CRITICAL
SDF9800
STDOFF-4.0OD3.5H-1.35-TH

CRITICAL
SDF9801
STDOFF-4.0OD3.5H-1.35-TH

APN 518S0671
CRITICAL
J9800
52893-8626
F-RT-SM

19D7 AUD_IPHS_SWITCH_EN
R9810 10K 5% 1/16W MF-LF 402
R9800 0 5% 1/16W MF-LF 402

21C3 21A4 AUD_I2C_INT_L
PULLUP ON PAGE 21
R9801 0 5% 1/16W MF-LF 402

52C6 =I2C_AUDIO_SCL
R9802 0 5% 1/16W MF-LF 402

52C6 =I2C_AUDIO_SDA
R9803 0 5% 1/16W MF-LF 402

17B6 AUD_IP_PERIPHERAL_DET
INTERNAL PULLUP IN MCP79 (P16)
R9804 0 5% 1/16W MF-LF 402

9A7 GND_AUDIO_SPKRAMP
C9800 1UF 10V 25V X7R 805

6A4 =PP12V_S0_AUDIO_SPKRAMP
98C4 6A4 =PP5V_S0_AUDIO
21D7 HDA_SDIN0
103B3 21D2 HDA_SDOUT
103B3 21D2 HDA_BIT_CLK
103B3 21D2 HDA_RST_L
103B3 21D2 HDA_SYNC
98C4 6B4 =PP3V3_S0_AUDIO

AUD_IPHS_SWITCH_EN_CONN
AUD_I2C_INT_L_CONN
I2C_AUDIO_SCL
I2C_AUDIO_SDA
AUD_IP_PERIPHERAL_DET_CONN
MIKEY SUPPORT

=PP5V_S0_AUDIO 6A4 98C6
=PP3V3_S0_AUDIO 6B4 98C6
NOSTUFF C9801 0.1UF 20% 10V CERM 402
NOSTUFF C9802 0.1UF 20% 10V CERM 402

CRITICAL
SDF9803
STDOFF-4.0OD3.5H-1.35-TH

CRITICAL
SDF9804
STDOFF-4.0OD3.5H-1.35-TH

STANDOFFS ARE 860-0893

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MLB: AUDIO CONNECTOR

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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D	051-7840	10
SCALE: NONE	SHT 98 OF 109	

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?
FSB_ADSTB	*	=2x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.
Signals within each 4x group should be matched within 5 ps of strobe.
DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 300 ps.
Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.
DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.

FSB 2X signals / groups shown in signal table on right.
Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 300 ps.
Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.
Signals within each 1x group should be matched to CPU clock, +0/-1000 mils.

Design Guide recommends each strobe/signal group is routed on the same layer.
Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	0.175 MM	0.175 MM

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	0.2 MM	?
CPU_COMP	*	0.6 MM	?
CPU_GTLREF	*	0.6 MM	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	0.6 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

SR DG recommends at least 25 mils, >50 mils preferred

MOST CPU SIGNALS WITH IMPEDANCE REQUIREMENTS ARE 50-OHM SINGLE-ENDED.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU / FSB Net Properties

	NET_TYPE			
	ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
FSB 4X Signal Groups	FSB_DATA_GROUP0_PP	FSB_50S	FSB_DATA	FSB_D_L<0> 7D7 7D8 10C4 14D3
	FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB_D_L<15..1> 10C4 14D3
	FSB_DATA_GROUP0_PP	FSB_50S	FSB_DATA	FSB_DINV_L<0> 7D7 7D8 10C4 14D6
	FSB_DSTB0_PP	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<0> 7D7 7D8 10C4 14D6
		FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<0> 10C4 14D6
	FSB_DATA_GROUP1_PP	FSB_50S	FSB_DATA	FSB_D_L<16> 7D7 7D8 10C4 14D3
	FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB_D_L<31..17> 10B4 10C4 14C3 14D3
	FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB_DINV_L<1> 10B4 14D6
	FSB_DSTB1_PP	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<1> 7D7 7D8 10B4 14D6
		FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<1> 10B4 14D6
	FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB_D_L<40..32> 10C2 14C3
	FSB_DATA_GROUP2_PP	FSB_50S	FSB_DATA	FSB_D_L<41> 7D7 7D8 10C2 14C3
	FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB_D_L<47..42> 10C2 14B3 14C3
	FSB_DATA_GROUP2_PP	FSB_50S	FSB_DATA	FSB_DINV_L<2> 7D7 7D8 10C2 14D6
	FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<2> 10C2 14D6
		FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<2> 7D7 7D8 10C2 14D6
	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_D_L<58..48> 10B2 10C2 14B3
	FSB_DATA_GROUP3_PP	FSB_50S	FSB_DATA	FSB_D_L<59> 7D7 7D8 10B2 14B3
	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_D_L<63..60> 10B2 14B3
	FSB_DATA_GROUP3_PP	FSB_50S	FSB_DATA	FSB_DINV_L<3> 7D7 7D8 10B2 14D6
	FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<3> 10B2 14D6
		FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<3> 7D7 7D8 10B2 14D6
FSB 2X Signals	FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB_A_L<5..3> 10D8 14D6
	FSB_ADDR_GROUP0_PP	FSB_50S	FSB_ADDR	FSB_A_L<6> 7D7 7D8 10D8 14D6
	FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB_A_L<16..7> 10D8 14C6 14D6
	FSB_ADDR_GROUP0_PP	FSB_50S	FSB_ADDR	FSB_REQ_L<4..0> 7C7 7C8 10D8 14B6
	FSB_ADSTB0_PP	FSB_50S	FSB_ADSTB	FSB_ADSTB_L<0> 7D7 7D8 10D8 14B6
	FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB_A_L<26..17> 10C8 10D8 14C6
	FSB_ADDR_GROUP1_PP	FSB_50S	FSB_ADDR	FSB_A_L<27> 7D7 7D8 10C8 14C6
	FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB_A_L<35..28> 10C8 14C6
	FSB_ADSTB1_PP	FSB_50S	FSB_ADSTB	FSB_ADSTB_L<1> 7D7 7D8 10C8 14B6
FSB 1X Signals	FSB_1X	FSB_50S	FSB_1X	FSB_ADS_L 10D6 14B6
	FSB_BREQ0_L_PP	FSB_50S	FSB_1X	FSB_BREQ0_L 7D7 10D6 14B6 23C3
		FSB_50S	FSB_1X	FSB_BREQ1_L 14B6
	FSB_1X_PP	FSB_50S	FSB_1X	FSB_BNR_L 7D7 10D6 14B6
	FSB_1X	FSB_50S	FSB_1X	FSB_BPRI_L 10D6 14B3
	FSB_1X_PP	FSB_50S	FSB_1X	FSB_DBSY_L 7D7 10D6 14B6
	FSB_1X	FSB_50S	FSB_1X	FSB_DEFER_L 10D6 14B3
	FSB_1X	FSB_50S	FSB_1X	FSB_DRDY_L 10D6 14B6
	FSB_1X_PP	FSB_50S	FSB_1X	FSB_HIT_L 7D7 10D6 14B6
	FSB_1X_PP	FSB_50S	FSB_1X	FSB_HITM_L 7D7 10D6 14B6
	FSB_1X_PP	FSB_50S	FSB_1X	FSB_LOCK_L 7D7 10D6 14B6
	FSB_CPURST_L	FSB_50S	FSB_1X	FSB_CPURST_L 14A3 23C3 10D6 13C2
	FSB_1X	FSB_50S	FSB_1X	FSB_RS_L<2..0> 14A6 10D6
	FSB_1X	FSB_50S	FSB_1X	FSB_TRDY_L 14B6 10D6
	CPU_ASYNC_PP	CPU_50S	CPU_AGTL	CPU_A20M_L 7D8 14A3 10C8
	MCP_BSEL	CPU_50S	CPU_AGTL	MCP_BSEL<2..0> 23B6 23C6
	CPU_ASYNC_R	CPU_50S	CPU_8MIL	CPU_FERR_L 10C8 14B7
	CPU_ASYNC_PP	CPU_50S	CPU_AGTL	CPU_IGNNE_L 7D8 14A3 10C8
	CPU_ASYNC_PP	CPU_50S	CPU_AGTL	CPU_INIT_L 7D8 14A3 10D6
	CPU_ASYNC_PP	CPU_50S	CPU_AGTL	CPU_INTR 7D8 14A3 10C8
	CPU_ASYNC_PP	CPU_50S	CPU_AGTL	CPU_NMI 7D8 14A3 10B8
	CPU_PROCHOT	CPU_50S	CPU_AGTL	CPU_PROCHOT_L 10C5 14B6 50B3
	CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD 14A3 7B4 10B2 13C7
	CPU_ASYNC_PP	CPU_50S	CPU_AGTL	CPU_SMI_L 7C8 14A3 10B8
	CPU_ASYNC_PP	CPU_50S	CPU_AGTL	CPU_STPCLK_L 7D8 14A3 10C8
	PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM_THRMTRIP_L 10C6 50B1 14B7
	FSB_CPUSLP_L	CPU_50S	CPU_AGTL	FSB_CPUSLP_L 14A3 10B2
		CPU_50S	CPU_AGTL	CPU_DPSLP_L 14A3 10B2
		CPU_50S	CPU_AGTL	CPU_DPRSTP_L 14A3 10B2 71C7
		CPU_50S	CPU_AGTL	FSB_DPWR_L 7C7 14A3 10B2
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_VDD 14A6
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_GND 14A6
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_VCC 14A6
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_GND 14A6
	FSB_CLK_CPU_PP	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P 7C8 14B3 10B6
		CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N 7C8 14B3 7B3 10B6
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_P 14B3 7A4 13C3
		CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_N 14B3 7A4 13C3
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_P 14A4
		CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_N 14A4
	CPU_IERR_L	CPU_50S	CPU_AGTL	CPU_IERR_L 10D6
	PM_DPRSLPVR	CPU_50S	CPU_AGTL	PM_DPRSLPVR 21C7 71C8
	(See above)	CPU_50S	CPU_AGTL	IMVP_DPRSLPVR 71C7
	CPU_GTLREF	CPU_50S	CPU_GTLREF	CPU_GTLREF 29B2 10B4
	CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<3> 10B3
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<2> 10B3
	CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<1> 10B3
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<0> 10B3
	XDP_TDI_K50	CPU_50S	CPU_ITP	XDP_TDI 13B3 7A4 10B6 10C6
	XDP_TDO_K50	CPU_50S	CPU_ITP	XDP_TDO 10C6 7A4 10B6 13B3
	XDP_TMS_K50	CPU_50S	CPU_ITP	XDP_TMS 13B3 7A4 10B6 10C6
	XDP_TCK_K50	CPU_50S	CPU_ITP	XDP_TCK 13B6 7A4 10A6 10C6
	XDP_TRST_L_K50	CPU_50S	CPU_ITP	XDP_TRST_L 13B3 7A4 10A6 10C6
	XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<4..0> 10C6 13C6 7B4
	XDP_BPM_L5	CPU_50S	CPU_ITP	XDP_BPM_L<5> 10C5 13C6 7B4
	(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP_CPURST_L 7A4 13C4
		CPU_50S	CPU_8MIL	IMVP6_VID<6..0> 12C1 71C7
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P 11B5 71A3
		CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N 11A5 71A3
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P 71A5
		CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N 71A5

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CPU/FSB Constraints

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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SIZE	DRAWING NUMBER	REV.
D	051-7840	10

SCALE: NONE SHT 100 OF 109

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_40S_VDD	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_70D_VDD	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	=3:1_SPACING	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR2:

DQ signals should be matched within 20 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.
All DQS pairs should be matched within 100 ps of clocks.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.
A/BA/cmd signals should be matched within 75 ps, no CLK matching requirement.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

DDR3:

DQ signals should be matched within 5 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, inter-pair matching shoulw be within 180 ps
No DQS to clock matching requirement.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.
A/BA/cmd signals should be matched within 5 ps of CLK pairs.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3
SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	Y	0.175 MM	0.175 MM	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3.4

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_P<1..0>	15B5 31C5 31C7
	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_N<1..0>	15B5 31C5 31C7
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_CKE<1..0>	15A5 31D5 31D7
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_CS_L<1..0>	15B5 31C5 31C7
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_ODT<1..0>	15B5 31C5
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_A<14..0>	15B5 15C5 31C5 31C7
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_BA<2..0>	15C5 31C5 31C7
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_RAS_L	15C5 31C5
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_CAS_L	15C5 31C7
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_WE_L	15C5 31C7
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_A_DQ<6..0>	15B7 31C2 31C4 31D2 31D4
MEM_A_DQ_BYTE0_PP	MEM_40S	MEM_DATA	MEM_A_DQ<7>	7C7 15B7 31C4
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_A_DQ<13..8>	15B7 31C2 31C4
MEM_A_DQ_BYTE1_PP	MEM_40S	MEM_DATA	MEM_A_DQ<14>	7C7 15B7 31C2
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_A_DQ<15>	15B7 31C4
MEM_A_DQ_BYTE2_PP	MEM_40S	MEM_DATA	MEM_A_DQ<16>	7C7 15B7 31B4
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_A_DQ<23..17>	15B7 15C7 31B2 31B4 31C2 31C4
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_A_DQ<24>	15C7 31C4
MEM_A_DQ_BYTE3_PP	MEM_40S	MEM_DATA	MEM_A_DQ<25>	7C7 15C7 31C4
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_A_DQ<31..26>	15C7 31C2 31C4
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_A_DQ<39..32>	15C7 31B5 31B7 31C5 31C7
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_A_DQ<46..40>	15C7 15D7 31B5 31B7
MEM_A_DQ_BYTE5_PP	MEM_40S	MEM_DATA	MEM_A_DQ<47>	7C7 15D7 31B7
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_A_DQ<55..48>	15D7 31B5 31B7
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_A_DQ<58..56>	15D7 31A7 31B5
MEM_A_DQ_BYTE7_PP	MEM_40S	MEM_DATA	MEM_A_DQ<59>	7C7 15D7 31A7
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_A_DQ<63..60>	15D7 31A5 31A7 31B7
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_A_DM<0>	15A7 31C4
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_A_DM<1>	15A7 31C2
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_A_DM<2>	15B7 31B4
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_A_DM<3>	15B7 31C2
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_A_DM<4>	15B7 31B5
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_A_DM<5>	15B7 31B7
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_A_DM<6>	15B7 31B5
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_A_DM<7>	15B7 31A7
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_P<0>	15D5 31C2
	MEM_70D	MEM_DQS	MEM_A_DQS_N<0>	15D5 31D2
MEM_A_DQS1_PP	MEM_70D	MEM_DQS	MEM_A_DQS_P<1>	7C7 15D5 31C4
	MEM_70D	MEM_DQS	MEM_A_DQS_N<1>	15D5 31C4
MEM_A_DQS2_PP	MEM_70D	MEM_DQS	MEM_A_DQS_P<2>	7C7 15D5 31B2
	MEM_70D	MEM_DQS	MEM_A_DQS_N<2>	15D5 31C2
MEM_A_DQS3_PP	MEM_70D	MEM_DQS	MEM_A_DQS_P<3>	7C7 15D5 31C4
	MEM_70D	MEM_DQS	MEM_A_DQS_N<3>	15D5 31C4
MEM_A_DQS4_PP	MEM_70D	MEM_DQS	MEM_A_DQS_P<4>	7B7 15D5 31B7
	MEM_70D	MEM_DQS	MEM_A_DQS_N<4>	15D5 31B7
MEM_A_DQS5_PP	MEM_70D	MEM_DQS	MEM_A_DQS_P<5>	7B7 15D5 31B5
	MEM_70D	MEM_DQS	MEM_A_DQS_N<5>	15D5 31B5
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_P<6>	15D5 31B7
	MEM_70D	MEM_DQS	MEM_A_DQS_N<6>	7B7 15D5 31B7
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_P<7>	15D5 31A5
	MEM_70D	MEM_DQS	MEM_A_DQS_N<7>	15D5 31A5
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_P<1..0>	15B1 32C5 32C7
	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_N<1..0>	15B1 32C5 32C7
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_CKE<1..0>	15A1 32D5 32D7
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_CS_L<1..0>	15B1 32C5 32C7
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_ODT<1..0>	15B1 32C5
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_A<14..0>	15B1 15C1 32C5 32C7
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_BA<2..0>	15C1 32C5 32C7
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_RAS_L	15C1 32C5
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_CAS_L	15C1 32C7
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_WE_L	15C1 32C7
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_B_DQ<5..0>	15B3 32C2 32D2 32D4
MEM_B_DQ_BYTE0_PP	MEM_40S	MEM_DATA	MEM_B_DQ<6>	7B7 15B3 32C4
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_B_DQ<7>	15B3 32C4
MEM_B_DQ_BYTE1_PP	MEM_40S	MEM_DATA	MEM_B_DQ<8>	7B7 15B3 32C4
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_B_DQ<15..9>	15B3 32C2 32C4
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_B_DQ<22..16>	15B3 15C3 32B2 32B4 32C2 32C4
MEM_B_DQ_BYTE2_PP	MEM_40S	MEM_DATA	MEM_B_DQ<23>	7B7 15C3 32B4
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_B_DQ<24>	15C3 32C4
MEM_B_DQ_BYTE3_PP	MEM_40S	MEM_DATA	MEM_B_DQ<25>	7B7 15C3 32C4
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_B_DQ<31..26>	15C3 32C2 32C4
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_B_DQ<37..32>	15C3 32B5 32B7 32C5 32C7
MEM_B_DQ_BYTE4_PP	MEM_40S	MEM_DATA	MEM_B_DQ<38>	7B7 15C3 32B7
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_B_DQ<39>	15C3 32B5
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_B_DQ<47..40>	15C3 15D3 32B5 32B7
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_B_DQ<55..48>	15D3 32B5 32B7
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_B_DQ<61..56>	15D3 32A7 32B5 32B7
MEM_B_DQ_BYTE7_PP	MEM_40S	MEM_DATA	MEM_B_DQ<62>	7B7 15D3 32A5
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_B_DQ<63>	15D3 32A5
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_B_DM<0>	15A3 32C4
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_B_DM<1>	15A3 32C2
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_B_DM<2>	15B3 32B4
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_B_DM<3>	15B3 32C2
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_B_DM<4>	15B3 32B5
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_B_DM<5>	15B3 32B7
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_B_DM<6>	15B3 32B5
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_B_DM<7>	15B3 32A7

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_P<0>	15D1 32C2
	MEM_70D	MEM_DQS	MEM_B_DQS_N<0>	15D1 32D2
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_P<1>	15D1 32C4
	MEM_70D	MEM_DQS	MEM_B_DQS_N<1>	15D1 32C4
MEM_B_DQS2_PP	MEM_70D	MEM_DQS	MEM_B_DQS_P<2>	7B7 15D1 32B2
	MEM_70D	MEM_DQS	MEM_B_DQS_N<2>	15D1 32C2
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_P<3>	15D1 32C4
	MEM_70D	MEM_DQS	MEM_B_DQS_N<3>	7B7 15D1 32C4
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_P<4>	15D1 32B7
	MEM_70D	MEM_DQS	MEM_B_DQS_N<4>	7B7 15D1 32B7
MEM_B_DQS5_PP	MEM_70D	MEM_DQS	MEM_B_DQS_P<5>	7B7 15D1 32B5
	MEM_70D	MEM_DQS	MEM_B_DQS_N<5>	7B7 15D1 32B5
MEM_B_DQS6_PP	MEM_70D	MEM_DQS	MEM_B_DQS_P<6>	7B7 15D1 32B7
	MEM_70D	MEM_DQS	MEM_B_DQS_N<6>	15D1 32B7
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_P<7>	15D1 32A5
	MEM_70D	MEM_DQS	MEM_B_DQS_N<7>	7B7 15D1 32A5
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_VDD	16C6
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_GND	16C6

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Memory Constraints

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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SIZE	DRAWING NUMBER	REV.
D	051-7840	10

SCALE: NONE SHT: 101 OF: 109

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	0.5 MM	?
MCP_PEX_COMP	*	0.2 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4x_DIELECTRIC	?
SATA_TERMP	*	0.2 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=3x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

NET_TYPE				
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
	PCIE_90D	PCIE	PEG_R2D_C_P<15..0>	9C6 86A7 86B7 86C7 86D7
	PCIE_90D	PCIE	PEG_R2D_C_N<15..0>	9C6 86A7 86B7 86C7 86D7
	PCIE_90D	PCIE	PEG_D2R_P<15..0>	7B7 86A1 86B1 86C1 86D1 9C6
	PCIE_90D	PCIE	PEG_D2R_N<15..0>	7B7 86A1 86B1 86C1 86D1 9C6
PEG_R2D	PCIE_90D	PCIE	MXM_PCIE_R2D_P<15..0>	86A5 86B5 86C5 86D5 84A8 84B8
	PCIE_90D	PCIE	MXM_PCIE_R2D_N<15..0>	86A5 86B5 86C5 86D5 84A8 84B8
PEG_D2R_MXM3	PCIE_90D	PCIE	MXM_PCIE_D2R_P<7..0>	84C8 86A4 86B4 86C4
PEG_D2R_MXM3_PP	PCIE_90D	PCIE	MXM_PCIE_D2R_P<8>	84C8 86C4
PEG_D2R_MXM3	PCIE_90D	PCIE	MXM_PCIE_D2R_P<15..9>	84B8 84C8 86C4 86D4
	PCIE_90D	PCIE	MXM_PCIE_D2R_N<15..0>	84B8 84C8 86A4 86B4 86C4 86D4
	PCIE_90D	PCIE	PCIE_MINI_R2D_P	34C6
	PCIE_90D	PCIE	PCIE_MINI_R2D_N	34C6
PCIE_MINI_R2D	PCIE_90D	PCIE	PCIE_MINI_R2D_C_P	17B3 34B8
	PCIE_90D	PCIE	PCIE_MINI_R2D_C_N	17B3 34C8
PCIE_MINI_D2R_PP	PCIE_90D	PCIE	PCIE_MINI_D2R_P	7C8 34C8 17B6
	PCIE_90D	PCIE	PCIE_MINI_D2R_N	7C8 34C8 17B6
	PCIE_90D	PCIE	PCIE_FW_R2D_P	7D6 41C3
	PCIE_90D	PCIE	PCIE_FW_R2D_N	7D6 41C3
PCIE_FW_R2D_PP	PCIE_90D	PCIE	PCIE_FW_R2D_C_P	17B3 41C1
	PCIE_90D	PCIE	PCIE_FW_R2D_C_N	17B3 41C1
PCIE_FW_D2R_PP	PCIE_90D	PCIE	PCIE_FW_D2R_P	7C8 41C1 17B6
	PCIE_90D	PCIE	PCIE_FW_D2R_N	7C8 41C1 17B6
	PCIE_90D	PCIE	PCIE_FW_D2R_C_P	41C3
	PCIE_90D	PCIE	PCIE_FW_D2R_C_N	41C3
MCP_PE0_REFCLK	CLK_PCIE_100D	CLK_PCIE	GPU_CLK100M_PCIE_P	9C6 87C5
	CLK_PCIE_100D	CLK_PCIE	GPU_CLK100M_PCIE_N	9C6 87C5 7C3
MCP_PE1_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	17C3 34C6
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	17C3 34C6
MCP_PE2_REFCLK_PP	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_P	7D6 17C3 41C2
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_N	7D6 17C3 41C2
MCP_HDMI_RSET	MCP_DV_COMP		MCP_HDMI_RSET	18A6 26C7
MCP_HDMI_VPROBE	MCP_DV_COMP		MCP_HDMI_VPROBE	18A6 26C7
MCP_PEX_CLK_COMP	MCP_50S	MCP_PEX_COMP	MCP_PEX_CLK_COMP	17A6
MCP_IFPAB_RSET	MCP_DV_COMP	MCP_PEX_COMP	MCP_IFPAB_RSET	18A3 26C6
MCP_IFPAB_VPROBE	MCP_50S	MCP_PEX_COMP	MCP_IFPAB_VPROBE	18A3 26C6
SATA_HDD_R2D	SATA_100D	SATA	SATA_HDD_R2D_C_P	20D6 45D5
	SATA_100D	SATA	SATA_HDD_R2D_C_N	20D6 45D5
	SATA_100D	SATA	SATA_HDD_R2D_P	45D7
	SATA_100D	SATA	SATA_HDD_R2D_N	45D7
SATA_HDD_D2R_PP	SATA_100D	SATA	SATA_HDD_D2R_P	7B8 45C5 20D6
	SATA_100D	SATA	SATA_HDD_D2R_N	7B8 45D5 20D6
	SATA_100D	SATA	SATA_HDD_D2R_C_P	45D7
	SATA_100D	SATA	SATA_HDD_D2R_C_N	45D7
SATA_ODD_R2D	SATA_100D	SATA	SATA_ODD_R2D_C_P	20D6 45C5
	SATA_100D	SATA	SATA_ODD_R2D_C_N	20D6 45C5
	SATA_100D	SATA	SATA_ODD_R2D_P	45C7
	SATA_100D	SATA	SATA_ODD_R2D_N	45C7
SATA_ODD_D2R_PP	SATA_100D	SATA	SATA_ODD_D2R_P	7B8 45C5 20D6
	SATA_100D	SATA	SATA_ODD_D2R_N	7B8 45C5 20D6
	SATA_100D	SATA	SATA_ODD_D2R_C_P	45C7
	SATA_100D	SATA	SATA_ODD_D2R_C_N	45C7
MCP_SATA_TERMP	MCP_50S	SATA_TERMP	MCP_SATA_TERMP	20A6
PM_SLP_S3_L			PM_SLP_S3_L	21C3 7B4 9D7
PM_SLP_S4_L			PM_SLP_S4_L	21C3 7B4 38D7 49C5 50C3 70D8

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MCP Constraints 1

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SCALE: NONE	SHT 102 OF 109	

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.8.

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	0.15 MM	?
CLK_LPC	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.9.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIAS	*	=STANDARD	0.2 MM	0.2 MM	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.11.1.

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.12.1.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.13.

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.14.

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
PCI_REQ0_L	PCI_55S	PCI	PCI_REQ0_L 7B3 19D2 19D7
PCI_REQ1_L	PCI_55S	PCI	PCI_REQ1_L 7B3 19D2 19D7
PCI_CLK33M_MCP	CLK_PCI_55S	CLK_PCI	PCI_CLK33M_MCP_R 19C5
	CLK_PCI_55S	CLK_PCI	PCI_CLK33M_MCP 19C5
LPC_AD	LPC_55S	LPC	LPC_AD<0> 19B3 49C8 51D5 7D4
LPC_AD_2PP	LPC_55S	LPC	LPC_AD<1> 7B8 7D6 19B3 49C8 51D5 7D4
LPC_AD	LPC_55S	LPC	LPC_AD<3..2> 19B3 49C8 51D4 7D4
	LPC_55S	LPC	LPC_AD_R<3..0> 19B5
LPC_FRAME_L	LPC_55S	LPC	LPC_FRAME_L 19C3 7D4 49C8 51D5
	LPC_55S	LPC	LPC_FRAME_PU 51C2
	LPC_55S	LPC	LPC_FRAME_R_L 19C5 51C1
LPC_RESET_L	LPC_55S	LPC	LPC_RESET_L 19C3 9D4
LPC_CLK33M	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC_R 19B3 9B4
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC 9B2 49C8
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS 9B2 7D4 51D4
MCP_SUS_CLK	CLK_LPC_55S	CLK_LPC	PM_CLK32K_SUSCLK_R 21B3 9B4
	CLK_LPC_55S	CLK_LPC	PM_CLK32K_SUSCLK 9B2 49C5
MCP_USB_RBIAS	MCP_USB_RBIAS		MCP_USB_RBIAS_GND 20C4
USB_EXT	USB_90D	USB	USB_EXTA_P 20D3 46A7
	USB_90D	USB	USB_EXTA_N 20D3 46A7
	USB_90D	USB	USB_PORT0_P 46A5
	USB_90D	USB	USB_PORT0_N 46A5
USB_EXT	USB_90D	USB	USB_EXTB_P 20C3 46B6
	USB_90D	USB	USB_EXTB_N 20C3 46B6
	USB_90D	USB	USB_PORT1_P 46B5
	USB_90D	USB	USB_PORT1_N 46B5
USB_EXT	USB_90D	USB	USB_EXTC_P 20C3 46B3
	USB_90D	USB	USB_EXTC_N 20C3 46B3
	USB_90D	USB	USB_PORT2_P 46B2
	USB_90D	USB	USB_PORT2_N 46B2
USB_EXT_MUXED	USB_90D	USB	USB_EXTD_P 20D3 46D5
	USB_90D	USB	USB_EXTD_N 20D3 46D5
	USB_90D	USB	USB_D_MUXED_P 46D4
	USB_90D	USB	USB_D_MUXED_N 46D4
	USB_90D	USB	USB_PORT3_P 46D3
	USB_90D	USB	USB_PORT3_N 46D3
USB_MINI	USB_90D	USB	USB_MINI_P 20D3 34B3
	USB_90D	USB	USB_MINI_N 20D3 34B3
USB_CAMERA	USB_90D	USB	USB_CAMERA_P 7B8 20D3 47B7
	USB_90D	USB	USB_CAMERA_N 7B8 20D3 47B7
	USB_90D	USB	USB_CAMERA_L_P 47B6
	USB_90D	USB	USB_CAMERA_L_N 47B6
USB_BT_PP	USB_90D	USB	USB_BT_P 7B8 20D3 47D4
	USB_90D	USB	USB_BT_N 7B8 20C3 47D4
USB_IR	USB_90D	USB	USB_IR_P 20D3 47B4
	USB_90D	USB	USB_IR_N 20D3 47B4
USB_IR	USB_90D	USB	USB_IR_L_P 47B3
	USB_90D	USB	USB_IR_L_N 47B3
SPI_CLK	MCP_50S	SPI	SPI_CLK_R 7B8 21B3 51A6 61C6
	MCP_50S	SPI	SPI_CLK 61C5
SPI_MOSI	MCP_50S	SPI	SPI_MOSI_R 21B3 51A6 61C2
	MCP_50S	SPI	SPI_MOSI 61C4
SPI_MISO	MCP_50S	SPI	SPI_MISO 7B8 51A6 61B2 21B3
	MCP_50S	SPI	SPI_MISO_R 61B4
SPI_CS0	MCP_50S	SPI	SPI_CS0_R_L 21B3 51C6
	MCP_50S	SPI	SPI_CS0_L 51C7
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK 21D2 98C6
	HDA_55S	HDA	HDA_BIT_CLK_R 21D4 21A7
HDA_RST_L	HDA_55S	HDA	HDA_RST_L 21D2 98C6
	HDA_55S	HDA	HDA_RST_R_L 21D4 21A7
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT 21D2 98C6
	HDA_55S	HDA	HDA_SDOUT_R 21D4 21A7
HDA_SYNC	HDA_55S	HDA	HDA_SYNC 21D2 98C6
	HDA_55S	HDA	HDA_SYNC_R 21D4 21A7

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MCP Constraints 2

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MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	0.2 MM	0.2 MM	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	0.3 MM	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

RTL8211CLGR (ETHERNET PHY) CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	0.6 MM	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_VDD	18C6
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_GND	18C6
MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	MCP_CLK25M_BUF0_R	18C3 38B3
	ENET_MII_55S	MCP_BUF0_CLK	RTL8211_CLK25M_CKXTAL1	38B2 37B6
ENET_MDIO	ENET_MII_55S	ENET_MII	ENET_MDIO	18C3 37B6
ENET_MDC	ENET_MII_55S	ENET_MII	ENET_MDC	18D3 37B6
ENET_RXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK	37C1 18D6
	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK_R	37C4
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RXD<0>	37C1 18D6
	ENET_MII_55S	ENET_MII	ENET_RXD_R<0>	37C4
ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET_RXD<3..1>	37C1 18D6
	ENET_MII_55S	ENET_MII	ENET_RXD_R<3..1>	37C4
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RX_CTRL	37B1 18D6
	ENET_MII_55S	ENET_MII	ENET_RXCTL_R	37B4
ENET_TXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK	18D3 37C7
ENET_TXD0	ENET_MII_55S	ENET_MII	ENET_TXD<0>	18D3 37C6
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<3..1>	18D3 37C6
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TX_CTRL	18D3 37B6
ENET_MDI	ENET_MDI_100D	ENET_MDI	ENET_MDI_P<3..0>	37B3 39C5 39C6 39C7 39C8
	ENET_MDI_100D	ENET_MDI	ENET_MDI_N<3..0>	37B3 39C5 39C6 39C7 39D8
	ENET_MDI_100D	ENET_MDI	ENET_MDI_T_P<3..0>	39C1 39A4 39A5
	ENET_MDI_100D	ENET_MDI	ENET_MDI_T_N<3..0>	39C1 39D1 39A4 39A5

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Ethernet Constraints

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FIT:

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
FW_0_TPA	FW_110D	FW_TP	FW_PORT0_TPA_P	42C2 43B5
	FW_110D	FW_TP	FW_PORT0_TPA_N	42C2 43C5
FW_0_TPB	FW_110D	FW_TP	FW_PORT0_TPB_P	42C2 43C5
	FW_110D	FW_TP	FW_PORT0_TPB_N	42C2 43C5

PORT 1 & 2 NOT USED

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FireWire Constraints

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NONE	105	109

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	SMB_55S	SMB	SMBUS_SMC_A_S3_SCL	52D2
	SMB_55S	SMB	SMBUS_SMC_A_S3_SDA	52D2
	SMB_55S	SMB	SMBUS_SMC_B_S0_SCL	52C5
	SMB_55S	SMB	SMBUS_SMC_B_S0_SDA	52C5
	SMB_55S	SMB	SMBUS_SMC_0_S0_SCL	52D5
	SMB_55S	SMB	SMBUS_SMC_0_S0_SDA	52D5
	SMB_55S	SMB	SMBUS_SMC_BSA_SCL	52C2
	SMB_55S	SMB	SMBUS_SMC_BSA_SDA	52C2
	SMB_55S	SMB	SMBUS_SMC_MGMT_SCL	106D3 52C2
	SMB_55S	SMB	SMBUS_SMC_MGMT_SDA	106D3 52C2
	SMB_55S	SMB	SMBUS_SMC_MGMT_SCL	106D3 52C2
	SMB_55S	SMB	SMBUS_SMC_MGMT_SDA	106D3 52C2
	SMB_55S	SMB	SMBUS_MCP_0_CLK	13B6 21C3 7A4 52D8
	SMB_55S	SMB	SMBUS_MCP_0_DATA	13B6 21C3 7A4 52D8

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SMC Constraints

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Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	Y	0.5 MM	0.5 MM	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

NET_TYPE				
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
DP_ML_MXM3	DP_100D	DISPLAYPORT	DP_EG_ML_P<3..0>	87B5 91B7 91C4 91C8
DP_ML_MXM3	DP_100D	DISPLAYPORT	DP_IG_ML_P<3..0>	9C6 91B7 91B8 91C4 91C8
	DP_100D	DISPLAYPORT	DP_EG_ML_N<3..0>	87B5 91B8 91C4 91C8 91D8
	DP_100D	DISPLAYPORT	DP_IG_ML_N<3..0>	9C6 91B8 91C8 91D4 91D8
DP_ML_MXM3	DP_100D	DISPLAYPORT	DP_ML_P<3..0>	9185 91C2 91C5 94B8 94C1 94C8
	DP_100D	DISPLAYPORT	DP_ML_N<3..0>	9185 91C2 91C5 91D5 94B8 94C1 94C8
DP_ML_MXM3	DP_100D	DISPLAYPORT	DP_ML_CONN_P<3..0>	94C4 94C5
	DP_100D	DISPLAYPORT	DP_ML_CONN_N<3..0>	94C4 94C5
DP_IG_AUX_CH	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_P	18B6 93C8
	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_N	18B6 93C8
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_AUX_CH_SW_P	93C6
	DP_100D	DISPLAYPORT	DP_AUX_CH_SW_N	93D5
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_AUX_CH_C_P	93B2 93C4 94C2
	DP_100D	DISPLAYPORT	DP_AUX_CH_C_N	93C2 93D4 94C2
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_EG_AUXCH_P	87A6 93B4
	DP_100D	DISPLAYPORT	DP_EG_AUXCH_N	87A6 93C4
LVDS_A_CLK_MXM3	LVDS_100D	GND	LVDS_IG_A_CLK_P	18B3 89B8
	LVDS_100D	GND	LVDS_IG_A_CLK_N	18B3 89B8
LVDS_A_DATA_MXM3	LVDS_100D	LVDS	LVDS_IG_A_DATA_P<3..0>	18B3 89B8 89C8 89D8
	LVDS_100D	LVDS	LVDS_IG_A_DATA_N<3..0>	18B3 89B8 89C8 89D8
LVDS_B_CLK_MXM3	LVDS_100D	GND	LVDS_IG_B_CLK_P	18B3 89C5
	LVDS_100D	GND	LVDS_IG_B_CLK_N	18B3 89C5
LVDS_B_DATA_MXM3	LVDS_100D	LVDS	LVDS_IG_B_DATA_P<3..0>	18B3 89A8 89C5 89D5
	LVDS_100D	LVDS	LVDS_IG_B_DATA_N<3..0>	18B3 89A8 89C5 89D5
LVDS_A_CLK_MXM3	LVDS_100D	LVDS	LVDS_EG_A_CLK_P	87D5 89B6
	LVDS_100D	LVDS	LVDS_EG_A_CLK_N	87D5 89B6
LVDS_A_DATA_MXM3	LVDS_100D	LVDS	LVDS_EG_A_DATA_P<3..0>	87D5 89B6 89C6 89D6 90A6 90A8
	LVDS_100D	LVDS	LVDS_EG_A_DATA_N<3..0>	87D5 89B6 89C6 89D6 90A6 90A8
LVDS_B_CLK_MXM3	LVDS_100D	LVDS	LVDS_EG_B_CLK_P	87D5 89C3
	LVDS_100D	LVDS	LVDS_EG_B_CLK_N	87D5 89C3
LVDS_B_DATA_MXM3	LVDS_100D	LVDS	LVDS_EG_B_DATA_P<3..0>	87D5 89A6 89C3 89D3 90A8 90B6
	LVDS_100D	LVDS	LVDS_EG_B_DATA_N<3..0>	87D5 89A6 89C3 89D3 90A6 90B8
	LVDS_100D	LVDS	LVDS_EG_A_CLK_L_P	89B5 90A8
	LVDS_100D	LVDS	LVDS_EG_A_CLK_L_N	89B5 90A6
	LVDS_100D	LVDS	LVDS_EG_B_CLK_L_P	89C2 90A8
	LVDS_100D	LVDS	LVDS_EG_B_CLK_L_N	89C2 90A6

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GRAPHICS CONSTRAINTS

SYNC_MASTER=K50 SYNC_DATE=09/03/2008

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SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
PPDDR_MEM	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM
MEM_CLK	PPDDR_MEM	*	PWR_P2MM
MEM_CMD	PPDDR_MEM	*	PWR_P2MM
MEM_CTRL	PPDDR_MEM	*	PWR_P2MM
MEM_DATA	PPDDR_MEM	*	PWR_P2MM
MEM_DQS	PPDDR_MEM	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	GND	*	GND_P2MM
CPU_COMP	GND	*	GND_P2MM
CPU_GTLREF	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM
FSB_DSTB	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	PWR	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
THERMAL	*	*	4:1_SPACING
SWITCHNODE	*	*	SWITCHNODE
THERMAL	PWR	*	PWR_P2MM
THERMAL	GND	*	GND_P2MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
THERM_DIFF	*	1:1_DIFFPAIR

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	TOP			0.1 MM	600 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_40S_VDD	TOP			0.1 MM	600 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D	TOP			0.1 MM	600 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
PCIE_90D	TOP				500 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
USB_90D	TOP				500 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP	TOP			0.1 MM	500 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MCP_MEM_COMP	TOP			0.1 MM	500 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MCP_MII_COMP	TOP			0.1 MM	500 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MCP_USB_RBIAS	TOP			0.1 MM	500 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP	*			0.25 MM	250 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S	BOTTOM			0.23 MM	100 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE

K50/K51 SPECIFIC NET PROPERTIES

NET_TYPE				
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
		PPDDR_MEM	=PP1V5_S3_MEM_A	6D3 31A5 31D7
		PPDDR_MEM	=PP1V5_S3_MEM_B	6D3 32A5 32D7
		SWITCHNODE	IMVP6_PHASE1	71D4 71A6
		SWITCHNODE	IMVP6_PHASE2	71C4 71A4
		SWITCHNODE	IMVP6_PHASE3	72C6 72A7
		SWITCHNODE	1V8_SW	80C5
		SWITCHNODE	1V05S5_SW	79C5
		SWITCHNODE	P1V05S0_PHASE	76C6
		SWITCHNODE	3V3S5_SW	76C3
		SWITCHNODE	5VS3_SW	73C5
		SWITCHNODE	MCPCORES0_PHASE	74C5
THERM_DIFF	THERM_DIFF	THERMAL	SNS_T_DP1_DN6	55A8 55D6 55D8
	THERM_DIFF	THERMAL	SNS_T_DN1_DP6	55A8 55D6 55D8
THERM_DIFF	THERM_DIFF	THERMAL	SNS_T_DP2_DN3	55A8 55C6 55C8
	THERM_DIFF	THERMAL	SNS_T_DN2_DP3	55A8 55C6 55C8
THERM_DIFF	THERM_DIFF	THERMAL	CPU_THERMD_P	10C6 55D4
	THERM_DIFF	THERMAL	CPU_THERMD_N	10C6 55D4
THERM_DIFF	THERM_DIFF	THERMAL	SNS_T_DP4_DN5	55A8 55B6 55B8
	THERM_DIFF	THERMAL	SNS_T_DN4_DP5	55A8 55B6 55B8
THERM_DIFF	THERM_DIFF	THERMAL	MCP_THMDIODE_P	21C3 55C4
	THERM_DIFF	THERMAL	MCP_THMDIODE_N	21C3 55C4
THERM_DIFF	THERM_DIFF	THERMAL	MCPTHMSNS_D2_P	55B3
	THERM_DIFF	THERMAL	MCPTHMSNS_D2_N	55B3
THERM_DIFF	THERM_DIFF	THERMAL	MXM_PWRSRC_SENSOR_P	53C4
	THERM_DIFF	THERMAL	MXM_PWRSRC_SENSOR_N	53C4
THERM_DIFF	THERM_DIFF	THERMAL	SENSE_12V_S0_P	53B3 53B4
	THERM_DIFF	THERMAL	SENSE_12V_S0_N	53B3 53B4
THERM_DIFF	THERM_DIFF	THERMAL	SENSE_12V_S5_P	53B3 53C4
	THERM_DIFF	THERMAL	SENSE_12V_S5_N	53B3 53C4
THERM_DIFF	THERM_DIFF	THERMAL	SENSE_1V5_S0_P	54D6
	THERM_DIFF	THERMAL	SENSE_1V5_S0_N	54D6
THERM_DIFF	THERM_DIFF	THERMAL	SNS_LCD_P	55C7
	THERM_DIFF	THERMAL	SNS_LCD_N	55C7
THERM_DIFF	THERM_DIFF	THERMAL	SNS_ODD_P	55D7
	THERM_DIFF	THERMAL	SNS_ODD_N	55D7
THERM_DIFF	THERM_DIFF	THERMAL	SNS_CPU_H_P	55B7
	THERM_DIFF	THERMAL	SNS_CPU_H_N	55B7
THERM_DIFF	THERM_DIFF	THERMAL	SNS_HDD_P	55D6
	THERM_DIFF	THERMAL	SNS_HDD_N	55D6
THERM_DIFF	THERM_DIFF	THERMAL	HDD_OOB_TEMP_FILT	55D6
THERM_DIFF	THERM_DIFF	THERMAL	SNS_AMB_P	55C6
	THERM_DIFF	THERMAL	SNS_AMB_N	55C6
THERM_DIFF	THERM_DIFF	THERMAL	SNS_MXM_P	55B6
	THERM_DIFF	THERMAL	SNS_MXM_N	55B6
THERM_DIFF	THERM_DIFF	THERMAL	MCPTHMSNS_FILT_P	55B4
	THERM_DIFF	THERMAL	MCPTHMSNS_FILT_N	55B4

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K50/K51 SPECIFIC CONSTRAINTS

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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K50/K51 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,BOTTOM	NO_TYPE,BGA_P1MM	MM	15.5.1

PHYSICAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	100 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.345 MM	0.085 MM	=STANDARD		
27P4_OHM_SE	*	Y	0.275 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.19 MM	0.085 MM	=STANDARD		
40_OHM_SE	*	Y	0.15 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.125 MM	0.085 MM	15 MM		
50_OHM_SE	*	Y	0.1 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.1 MM	0.085 MM	=STANDARD		
55_OHM_SE	*	Y	0.075 MM	0.075 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3,ISL6	Y	0.155 MM	0.085 MM	=STANDARD	0.135 MM	0.1 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.185 MM	0.085 MM	=STANDARD	0.125 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL6	Y	0.099 MM	0.085 MM	12 MM	0.200 MM	0.1 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.121 MM	0.085 MM	=STANDARD	0.18 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL6	Y	0.081 MM	0.085 MM	=STANDARD	0.25 MM	0.1 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.085 MM	=STANDARD	0.180 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	TOP,BOTTOM	Y	0.085 MM	0.085 MM	=STANDARD	0.3 MM	0.15 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.085 MM
1:1_DIFFPAIR	TOP,BOTTOM	Y	=STANDARD	=STANDARD	=STANDARD	0.125 MM	0.085 MM

SPACING RULE SET

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SPACING_0.5MM	*	0.5 MM	?
CLK_SPACING_0.6MM	*	0.6 MM	?
GND_P2MM	*	0.2 MM	1000
PWR_P2MM	*	0.2 MM	1000
SWITCHNODE	*	0.6 MM	1000

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.150 MM	?
2X_DIELECTRIC	TOP,BOTTOM	0.160 MM	?
3X_DIELECTRIC	*	0.220 MM	?
3X_DIELECTRIC	TOP,BOTTOM	0.240 MM	?
4X_DIELECTRIC	*	0.300 MM	?
4X_DIELECTRIC	TOP,BOTTOM	0.320 MM	?
5X_DIELECTRIC	*	0.380 MM	?
5X_DIELECTRIC	TOP,BOTTOM	0.400 MM	?

CONSTRAINTS FOR BGA AREA

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	0.2 MM	?
BGA_P3MM	*	0.3 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_P1MM	BGA_P1MM
MEM_CLK	*	BGA_P1MM	BGA_P2MM
CLK_FSB	*	BGA_P1MM	BGA_P2MM
CLK_PCIE	*	BGA_P1MM	BGA_P1MM
FSB_DSTB	FSB_DSTB	BGA_P1MM	BGA_P1MM
CLK_LPC	*	BGA_P1MM	BGA_P1MM
CLK_PCI	*	BGA_P1MM	BGA_P1MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MCP_FSB_COMP	*	BGA_P1MM	BGA_P2MM
MCP_MEM_COMP	*	BGA_P1MM	BGA_P2MM
MCP_PEX_COMP	*	BGA_P1MM	BGA_P2MM
MCP_HDA_COMP	*	BGA_P1MM	BGA_P2MM

CONSTRAINTS ARE BASED ON MCP79 DESIGN GUIDE DG-03328-001_V06
PCI,LPC,SMB,HDA,SPI,RGMII,SMBUS ARE ROUTED AS 55 OHM SE SIGNALS

K50/K51 RULE DEFINITIONS

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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